Page Zero Implementation for EDUC–8

by

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A severe program limitation of the EDUC–8 is the inability to reference page 0 for memory reference instructions AND, TAD, ISZ and DCA. For example, say that a variable is used as the address for other areas in memory. This requires indirect addressing, with the variable having to be in the same 16 word page as the instruction. This means that if the variable is indirectly accessed in two different pages in a loop, then the variable must be copied back and forth between the pages if it is modified. This also makes programming difficult as care needs to be made so that the variable is in the same page as the indirect instruction.

The DEC PDP–8 computer solved this problem by having the fifth most significant bit or MSB (the three most significant bits had the op–code and the fourth MSB has the indirect addressing or I bit) be a page zero or Z bit. When 0 this refers to page zero and when 1 this refers to the current page. The remaining 12–5 = 7 bits refer to the location in the 128 12–bit word page. Thus, by having the variable in page zero this allows reference to that variable from multiple pages. Also, common constants that are used across many pages only need one location in page zero.

Implementing a Z bit in the EDUC–8 would reduce the page size from 16 to 8, which would make programming inefficient. In a page instructions either require one word for OPR, IOT or direct JMP and JMS instructions or two words for AND, TAD, ISZ, DCA or indirect JMP and JMS instructions. For these memory instructions we have one word for the instruction and one word for the address location. Thus, in a page there will never be more than eight addresses that are being accessed (either directly or indirectly).

Thus we propose the fifth MSB be used as a Z bit, but with a slight difference to that used in the PDP–8. In this case if the Z bit is 0, then only the first 8 locations in page zero are referenced. If the Z bit is 1, this refers to the upper 8 locations in the current page. As direct JMP and JMS instructions need to be able to access all locations in a page, then the fifth MSB is a normal address bit. There will also be no need to directly JMP or JMS to the first 8 page zero locations, as they will normally be used for variables and constants. In order to return from subroutines, JMP I also needs to access all locations in a page. JMS I can have the ability to refer to page 0.

In EDUC–8, during the FETCH or F cycle the PC address is copied to MA[7:0], which is then used to read the instruction from the RAM into MB[7:0]. During T23 of the F cycle, bits MA[7:4] are copied to MB[7:4] if the instruction is a memory reference instruction. Thus MB[7:4] contains the current page with MB[3:0] containing the 4–bit address of the instruction. To implement the Z bit, we need to force MB[7:4] low if F.T23 is high, MB3 is low (the Z bit), and we have either an AND, TAD, ISZ, DCA, or JMS I instruction. The MB3 = Z bit does not need to be changed as that will correctly refer to the lower half of page zero if 0 or the upper half of the current page if 1.

Fortuitously, a 9322 or 74157 multiplexer is used before the 7495 register for MB[7:4] in the E8M board. This has an $\overline{E}$ input which is tied low. However, when $\overline{E}$ is high, this will force the 74157 output low. Thus we need to make

$$\overline{E} = F.T23.\overline{MB3}.(AND + TAD + ISZ + DCA + JMS.MB4).$$

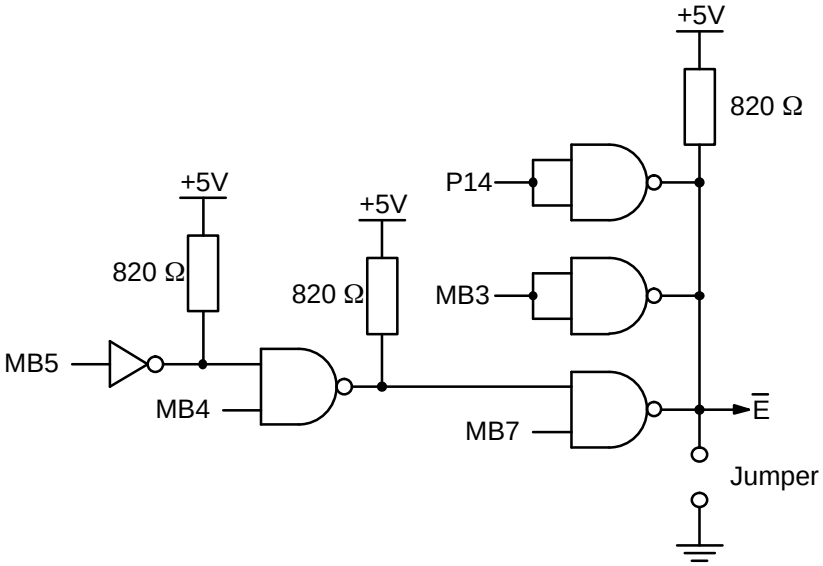
We have that pin 14 of the E8M board is equal to

$$P14 = \overline{F.T23.(\overline{OPR + IOT})} = \overline{F.T23.(AND + TAD + ISZ + DCA + JMP + JMS)}.$$

Thus, we have that

$$\begin{aligned}\overline{E} &= \overline{P14}.\overline{MB3}.(AND + TAD + ISZ + DCA + JMS.MB4)\\ &= \overline{P14}.\overline{MB3}.(\overline{MB7} + \overline{MB5}.MB4)\\ &= \overline{P14}.\overline{MB3}.(\overline{MB7.\overline{\overline{MB5}.MB4}}).\end{aligned}$$

We can implement this using the following circuit:



Parts List
1 7401 quad OC NAND
1/6 7405 hex OC INV
3 820 Ω resistors
1 Jumper

Note: Inverter uses pins 3 and 4 of 7405 at E8M row 2 column 6. Need to cut tracks so that track from pin 1 goes around pin 3, instead of through pin 3.

This design only requires one additional 7401 quad open collector NAND and three 820 Ω resistors. An additional inverter is a spare from the existing design. With the jumper in place, the original EDUC–8 instruction set is used.

Note that there is an error in Figure 3 showing the E8M schematic. The NAND gate that has $\overline{ISZ}$ (C) and $\overline{F.T23.(\overline{OPR + IOT})}$ (14) as inputs, should have $\overline{ISZ}$ (C) and $\overline{DEP}$ (19) as inputs.