

* = New Connection

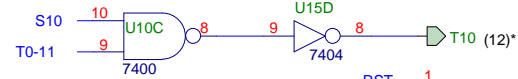
E8/T Modifications

Signal labels FETCH_CYC and EXECUTE_CYC are incorrect.

They should be labelled T0-11 and T12-23.

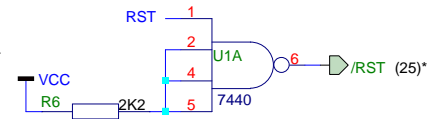
Disconnect S2-9 and T12-23 from U10C.

Signal T14-21_2 becomes T10. Total UL for T14-21_1 goes from 2 to 4.



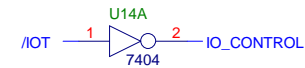
For 74 series only, replace U20 with 74H04 or 74S04.

For 74 series only, replace U1 with 7440.



E8/D Modifications

U7C needs to be replaced with spare gate U14A.



(was U7C)

Signal labels /(Q7+EXEC.MB4) and /(Q7+EXEC).MB4 are incorrect.

They should be labelled EXEC.Q7./MB4 and EXEC.Q7.MB4.

U14B, U14C and U2A are spare gates. New part is U15 7420.

U10 and U11 7400 need to be deleted and replaced with 7410 as to left.

Disconnect T14-21-1 from (10) and connect T14-21 to T14-21-1.

LO = EXEC.Q7./MB4

HI = EXEC.Q7.MB4

CLA = LO.MB3./MB1

CMA = LO.MB2./MB1

RAL = LO.MB1./MB2./MB3

IAC = LO.MB0./MB1

CLL = LO.MB3.MB1

CML = LO.MB2.MB1

SZA = HI.MB3

SMA = HI.MB2

RAR = HI.MB1./MB2./MB3

HLT = HI.MB0./MB1

List of New Instructions

703 RLL (rotate link left through AC register)

707 CML (complement link)

713 CLL (clear link)

717 CLL.CML (set link)

723 RLR (rotate link right through AC register)

727 SNL (skip on negative link)

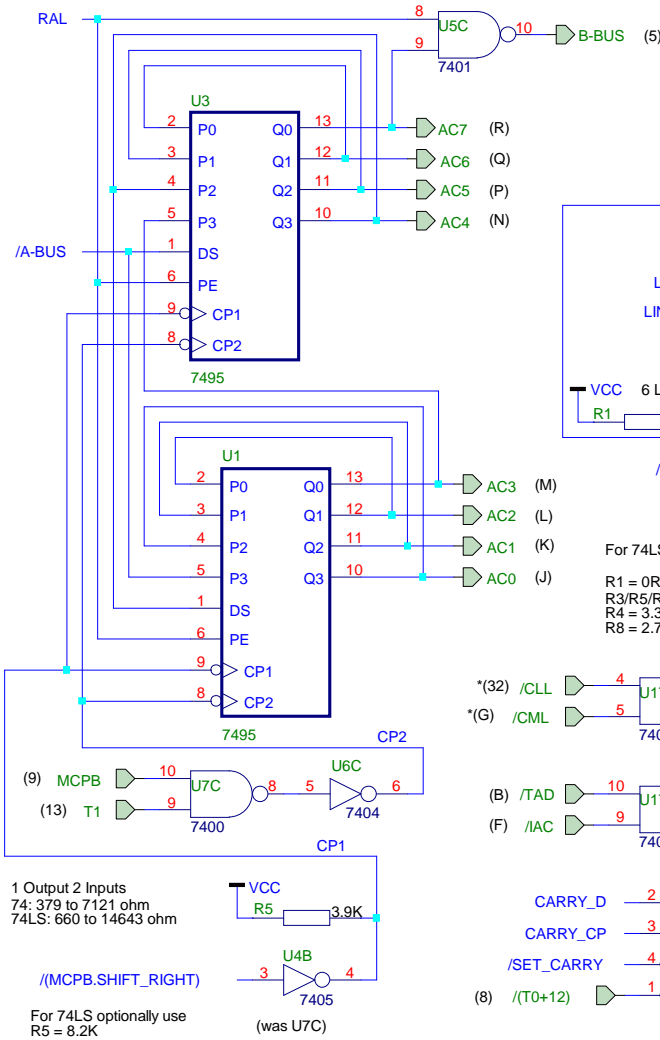
733 SZL (skip on zero link)

737 SZL.SNL (skip)

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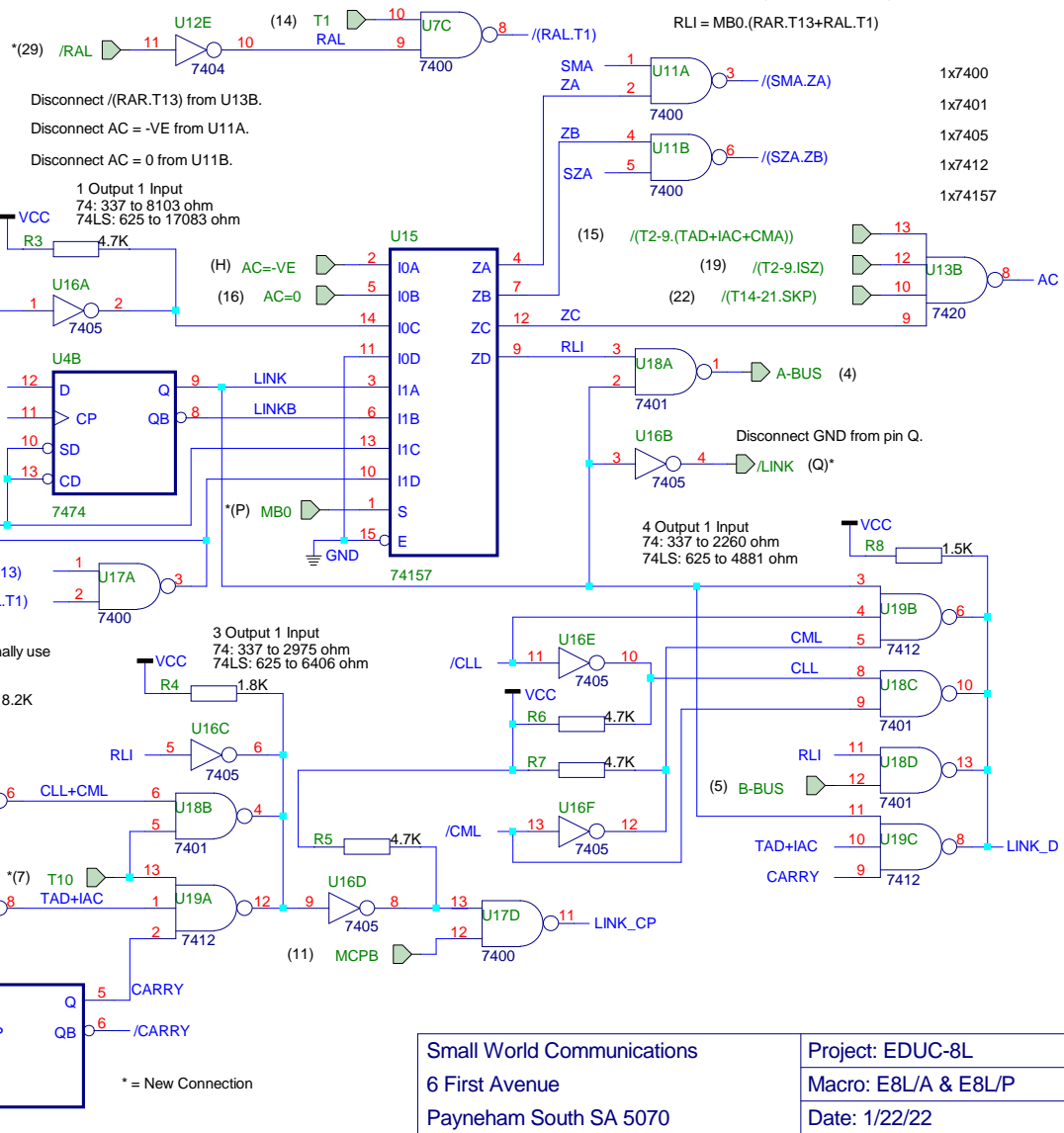
E8/A Modifications

- U7C needs to be replaced with spare gate U4B.
- Disconnect AC7 from U1.P3
- Disconnect T1 from U1./CP2 and U3./CP2.
- Disconnect RAL from U6C.
- U4B, U5C and U6C are spare gates.



E8/P Modifications

- Disconnect /(T14-21.(JMP+JMS)) from U12E.
- U7C and U12E are spare gates. U4B is spare FF.



$$\begin{aligned}
 ZA &= \text{/MB0.(AC=-VE)} + \text{MB0.LINK} \\
 ZB &= \text{/MB0.(AC=0)} + \text{MB0./LINK} \\
 ZC &= \text{MB0} + \text{/(RAR.T13+RAL.T1)} \\
 \text{RLI} &= \text{MB0.(RAR.T13+RAL.T1)}
 \end{aligned}$$

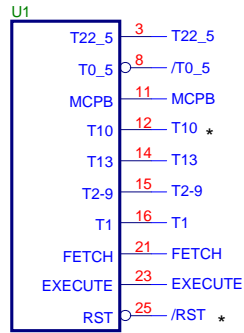
N

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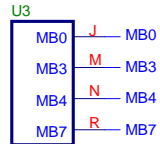
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E8/C Modifications

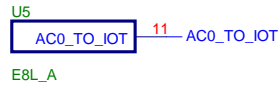
Disconnect T14-21 from pin E8/T(12).



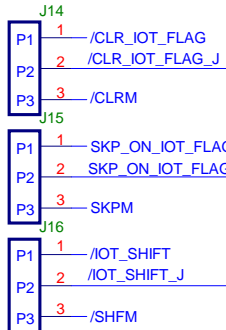
E8L_T



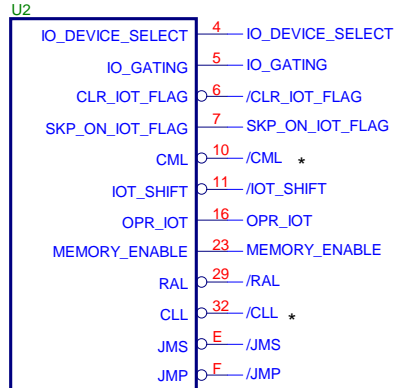
E8_M



E8L_A

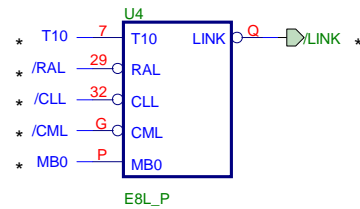


Disconnect T14-21 from pin E8/D(10).
Disconnect GND from pin E8/D(32).



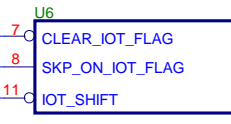
E8L_D

Disconnect D-BUS from pin E8/P(7).
Disconnect GND from pin E8/P(32).
Disconnect GND from pin E8/P(Q).



E8L_P

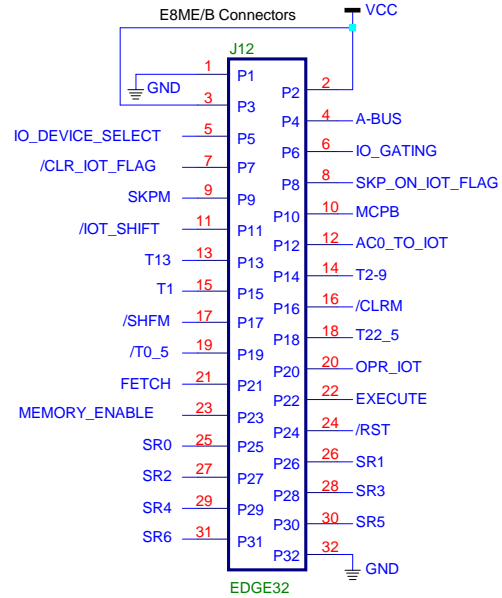
Disconnect /CLEAR_IOT_FLAG from pin E8/IOT(7).
Disconnect SKP_ON_IOT_FLAG from pin E8/IOT(8).
Disconnect /IOT_SHIFT from pin E8/IOT(11).



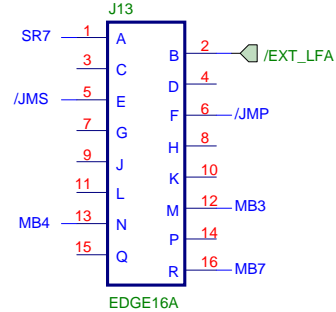
E8L_IOT

Jumpers in upper position (A-B) without EDUC-8ME.
Jumpers in lower position (B-C) with EDUC-8ME.

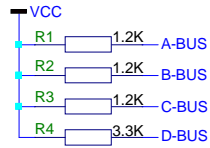
* = New Connection



EDGE32



EDGE16A



No=2, Iol=0.1mA, Vol=0.45 V: 74 li = 3/3 UL: 429 to 7334 ohm;

For 74LS optionally use

R1/R2 = 2.2K
R3 = 1.8K
R4 = 4.7K

No=5, 74 li = 3/3 UL: 433 to 1715 ohm; 74LS li = 1.5/0.75 UL: 699 to 3661 ohm

No=6, 74 li = 1.4/2 UL: 379 to 1510 ohm; 74LS li = 0.9/1.25 UL: 792 to 3223 ohm

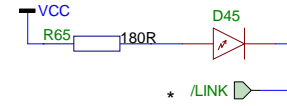
No=6, 74 li = 2.4/3 UL: 433 to 1472 ohm; 74LS li = 1.4/1.5 UL: 848 to 3125 ohm

No=1, 74 li = 3/3 UL: 433 to 6351 ohm; 74LS li = 1.5/0.75 UL: 699 to 12812 ohm

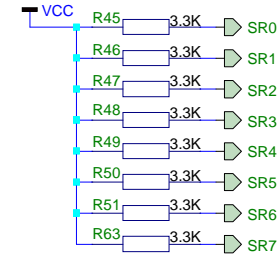
74LS li = 1.5/0.75 UL: 324 to 7885 ohm (EDUC-8)

E8/F Modifications

Add LED for LINK next to AC7.



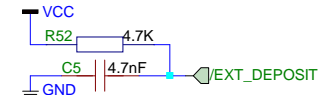
Replace EDUC-8 E8/F 10K SR pullups with 3.3K resistors.
For 74 with 1 output and 3 inputs: 433 to 6351 ohms
For 74LS with 1 output and 3 inputs: 699 to 12812 ohms
For 74LS optionally use 6.8K pullups.



For paper tape reader C5 needs to be changed.
See Electronics Australia, March 1975, page 66.
Have R = 22K and C = 1 nF, RC = 22 us.

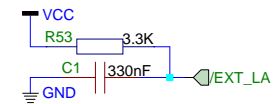
For 74 with 1 output and 1 input: 337 to 8103 ohm.
For 74LS with 1 output and 1 input: 625 to 17083 ohm.
Choose R = 4.7K and C = 4.7 nF, RC = 22.09 us.

For 74LS optionally use
R52 = 8.2K
C5 = 2.7nF
RC = 22.14 us



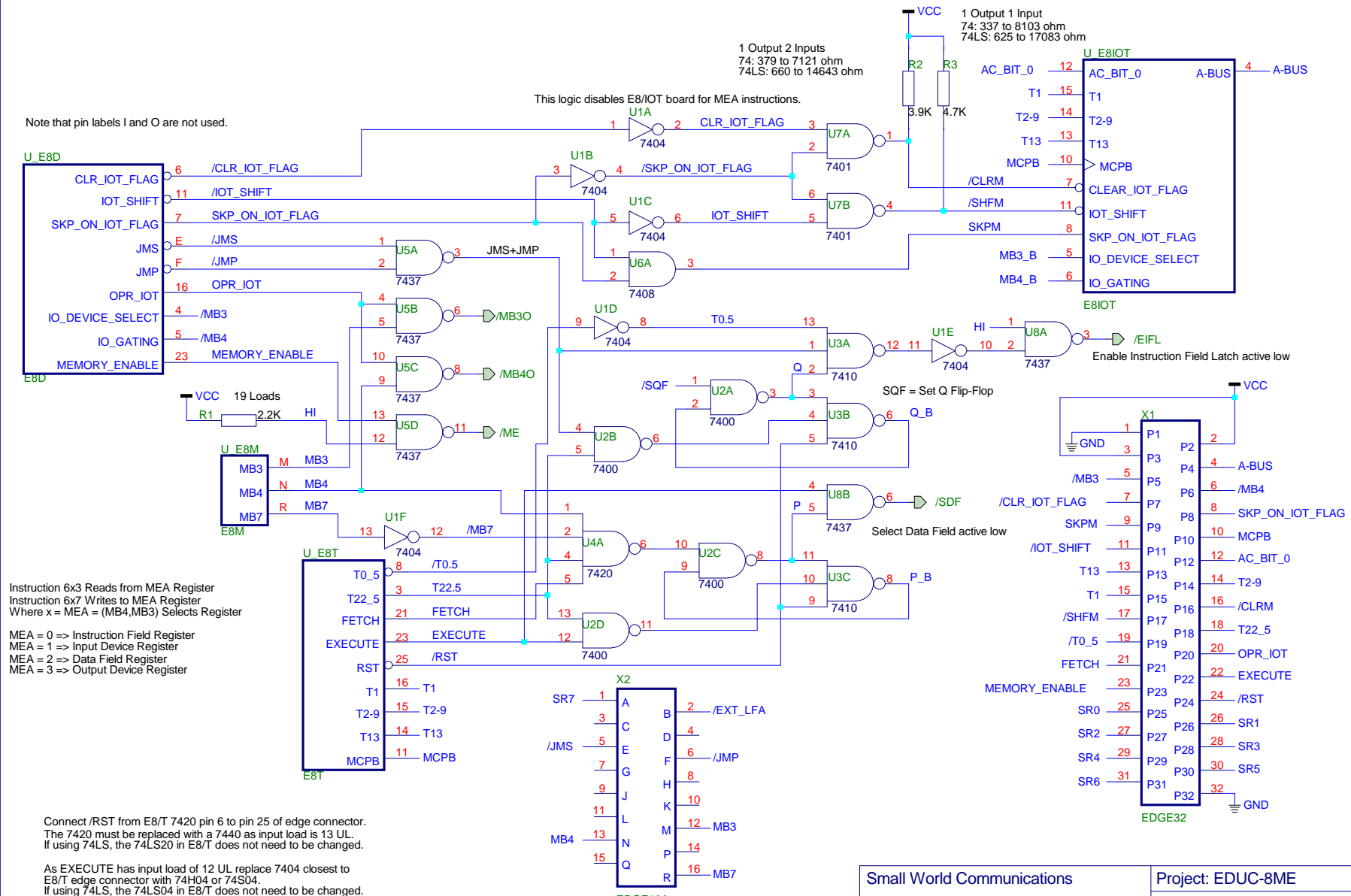
For /EXT_LA have R = 10 K and C = 100 nF, RC = 1 ms.
For 74 with 1 output and 2 inputs: 379 to 7121 ohm.
For 74LS with 1 output and 2 inputs: 660 to 14643 ohm.
Choose R = 3.3K and C = 330 nF, RC = 1.089 ms.

For 74LS optionally use
R53 = 8.2K
C1 = 120nF
RC = 0.984 ms



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Note that pin labels I and O are not used.

U_E8D

6	/CLR_IOT_FLAG
11	/IOT_SHIFT
7	SKP_ON_IOT_FLAG
E	/JMS
F	/JMP
16	OPR_IOT
4	/MB3
5	/MB4
23	MEMORY_ENABLE

VCC 19 Loads

U_E8M

M	MB3
N	MB4
R	MB7

U_E8T

8	/T0.5
3	T22.5
21	FETCH
23	EXECUTE
25	/RST
16	T1
15	T2-9
14	T13
11	MCPB

This logic disables E8/IOT board for MEA instructions.

1 Output 2 Inputs
74: 379 to 7121 ohm
74LS: 660 to 14643 ohm

1 Output 1 Input
74: 337 to 8103 ohm
74LS: 625 to 17083 ohm

Instruction 6x3 Reads from MEA Register
Instruction 6x7 Writes to MEA Register
Where x = MEA = (MB4,MB3) Selects Register

MEA = 0 => Instruction Field Register
MEA = 1 => Input Device Register
MEA = 2 => Data Field Register
MEA = 3 => Output Device Register

Connect /RST from E8/T 7420 pin 6 to pin 25 of edge connector.
The 7420 must be replaced with a 7440 as input load is 13 UL.
If using 74LS, the 74LS20 in E8/T does not need to be changed.

As EXECUTE has input load of 12 UL replace 7404 closest to
E8/T edge connector with 74H04 or 74S04.
If using 74LS, the 74LS04 in E8/T does not need to be changed.

X2

1	A	2	/EXT_LFA
3	C	4	
5	E	6	/JMP
7	G	8	
9	J	10	
11	L	12	MB3
13	N	14	
15	Q	16	MB7

X1

1	P1	2	
3	P3	4	A-BUS
5	P5	6	/MB4
7	P7	8	SKP_ON_IOT_FLAG
9	P9	10	MCPB
11	P11	12	AC_BIT_0
13	P13	14	T2-9
15	P15	16	/CLR_M
17	P17	18	T22_5
19	P19	20	OPR_IOT
21	P21	22	EXECUTE
23	P23	24	/RST
25	P25	26	SR1
27	P27	28	SR3
29	P29	30	SR5
31	P31	32	

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Parts List

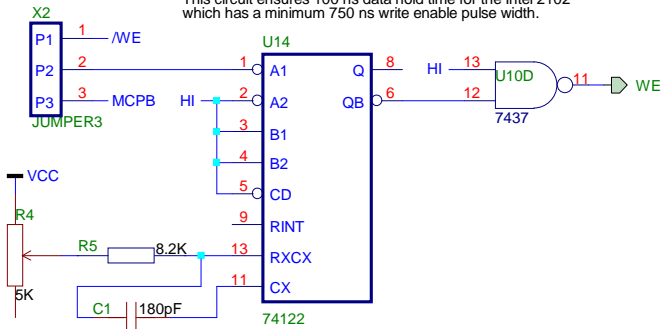
- 1 7400 quad 2-input NAND
- 1 7401 quad 2-input NAND OC
- 1 7404 hex inverter
- 1 7408 quad 2-input AND
- 1 7410 triple 3-input NAND
- 1 7411 triple 3-input NAND
- 1 7420 dual 4-input NAND
- 6 7437 quad 2-input NAND driver
- 1 74122 multivibrator
- 1 2.2K resistor
- 1 3.9K resistor
- 1 4.7K resistor
- 1 8.2K resistor
- 1 5K trimpot
- 1 180 pF capacitor
- 1 3-pin jumper
- 1 16-pin socket
- 1 16-way edge connector
- 1 32-way edge connector
- 1 40-way IDC connector

For 74LS optionally use

R1 = 0R
R2/R3 = 8.2K

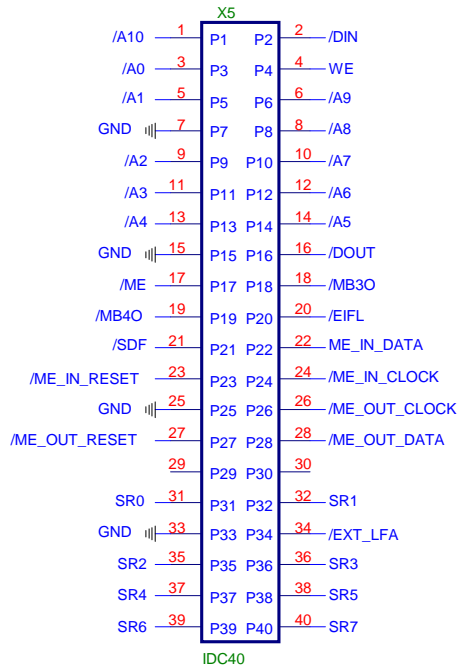
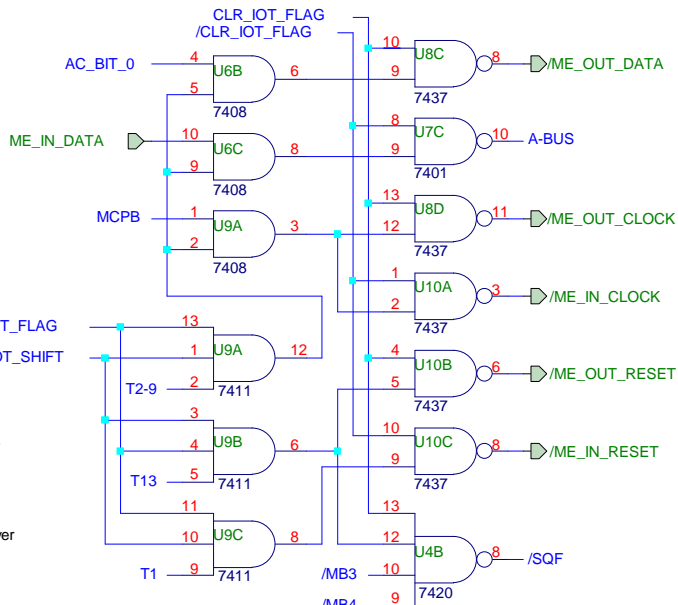
For 74LS122 use C1 = 150pF

This circuit ensures 100 ns data hold time for the Intel 2102 which has a minimum 750 ns write enable pulse width.

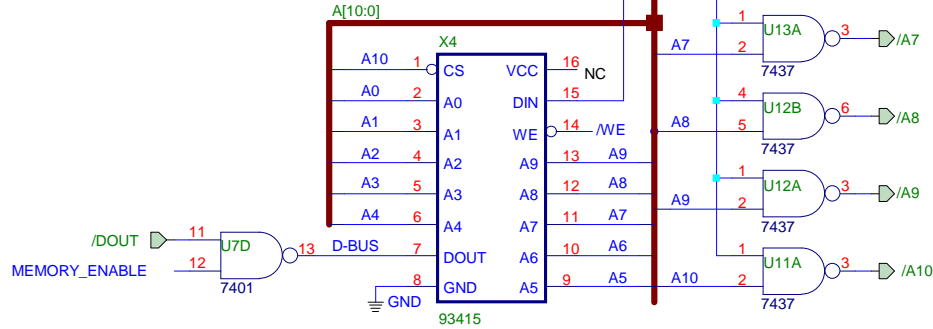


For normal operation jumper pins 1 and 2 of X2.

To adjust WE pulse width, disconnect EDUC-8ME and cable from E8/M. Insert 93415 into lower position of E8/M and jumper pins 2 and 3 of X2. Load instruction JMP 0 (500) into address 000 and run program. Adjust trimpot R4 so that the low width of QB is at least 750 ns and at most Tch-132 ns where Tch is the MCPB high width in ns.

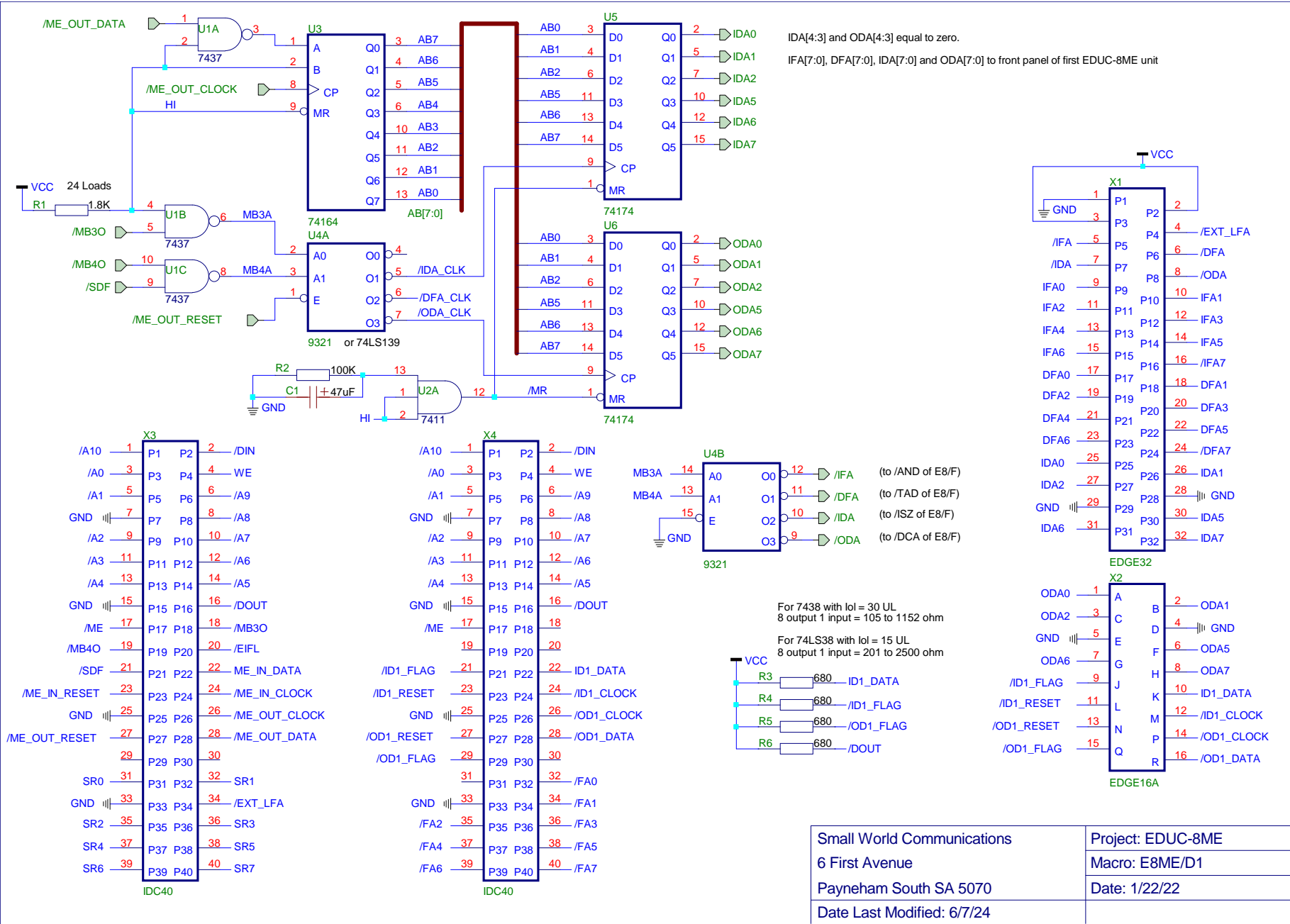


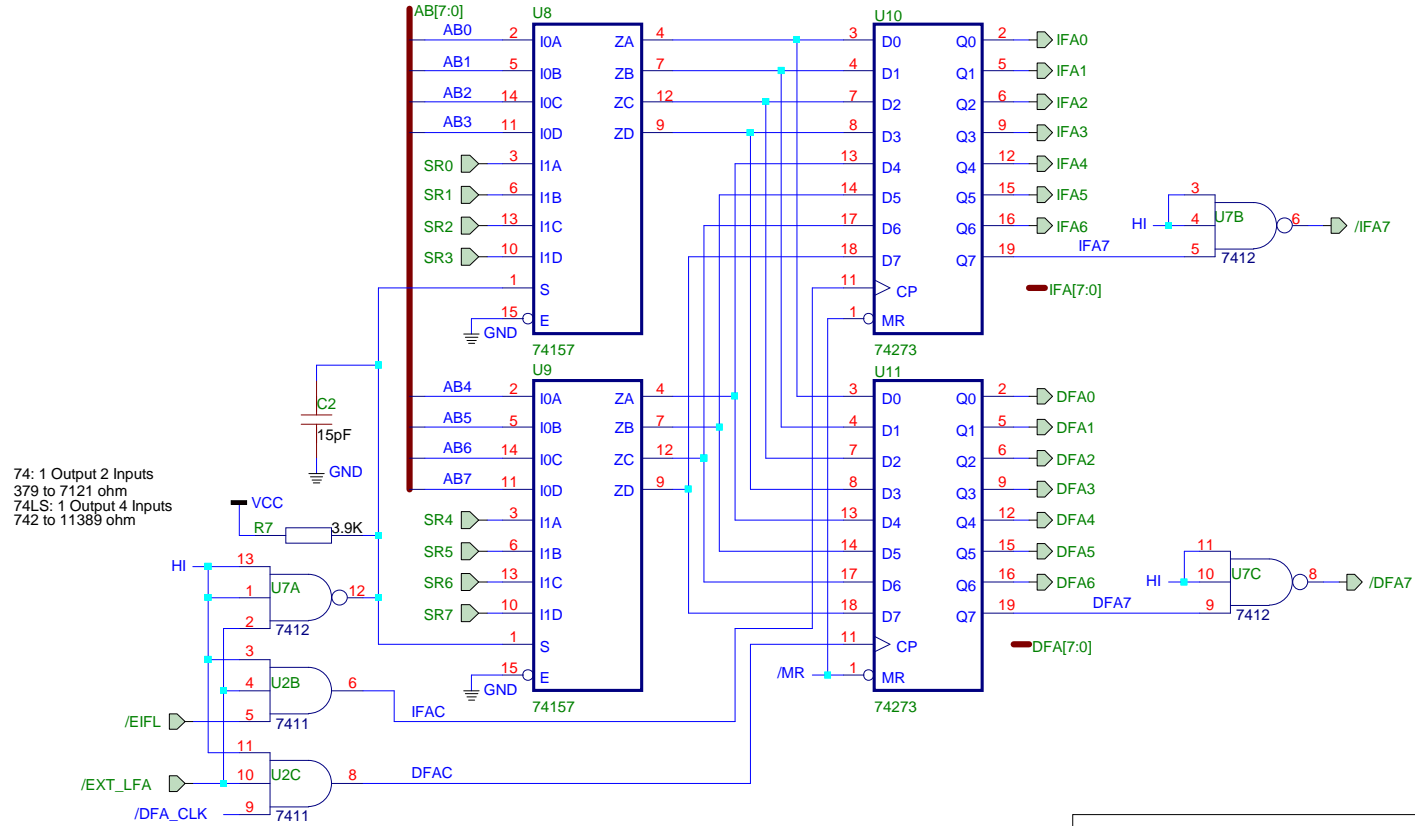
Connect cable from X4 to lower memory position of E8/M. VCC of X2 must not be connected to board power supply.



Use HI for unused gate inputs to reduce power

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74: 1 Output 2 Inputs
 379 to 7121 ohm
 74LS: 1 Output 4 Inputs
 742 to 11389 ohm

Parts List

- 1 7411 triple 3-input AND
- 1 7412 triple 3-input NAND OC
- 3 7437 quad 2-input NAND buffer
- 1 74139/932 1 dual 2 to 4 decoder
- 4 74153 dual 4 to 1 multiplexer
- 2 74157 quad 2 to 1 multiplexer
- 1 74164 8-bit S/P shift register
- 1 74165 8-bit P/S shift register
- 2 74174 6-bit D-FF
- 2 74273 8-bit D-FF
- 4 680R resistors
- 1 3.9K resistor
- 1 100K resistor
- 1 15 pF capacitor
- 1 47 uF capacitor
- 1 16-way edge connector
- 1 32-way edge connector
- 2 40-way IDC connectors

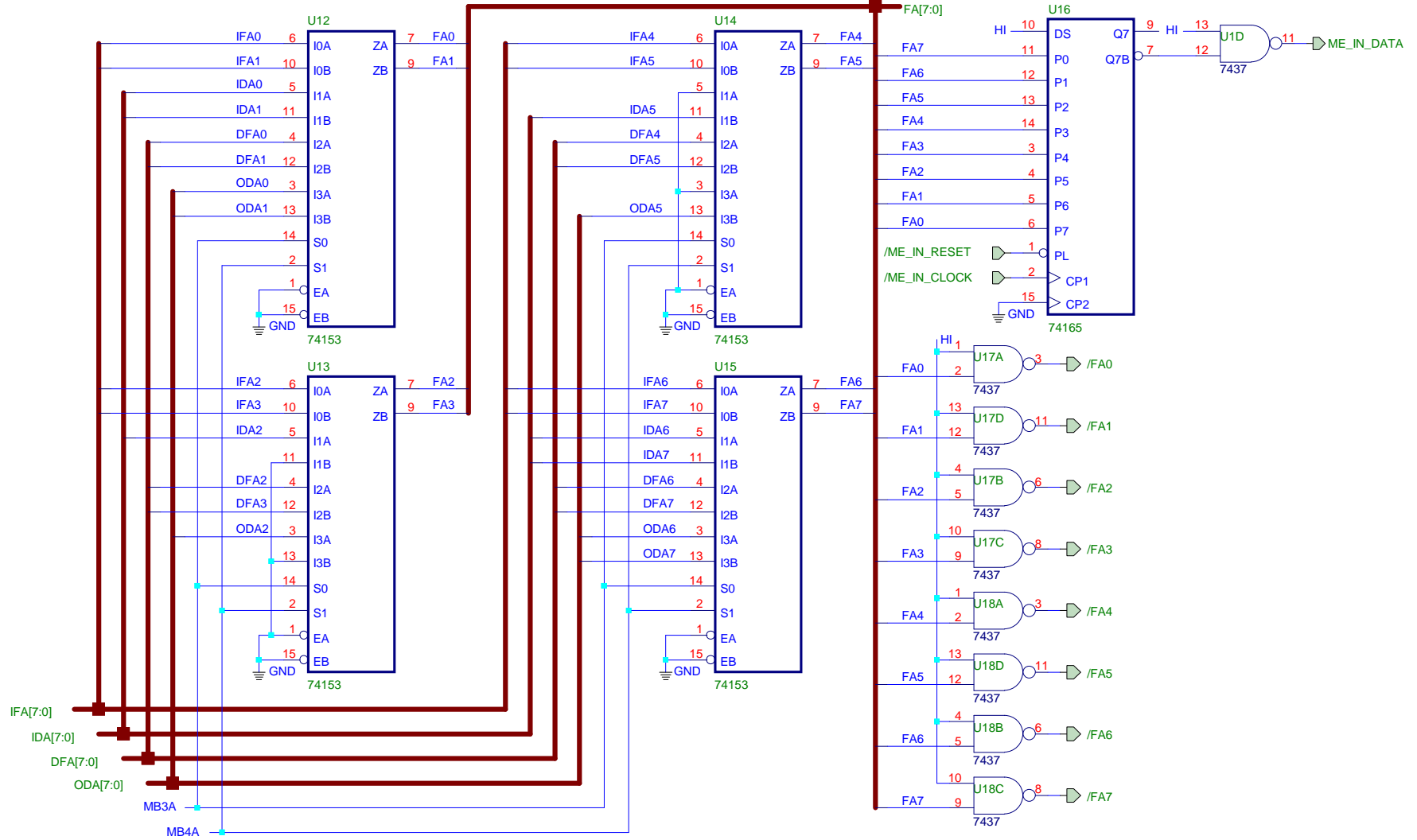
For 74LS optionally use

- R1 = 0R
- R3 to R6 = 1.5K
- R7 = 5.6K

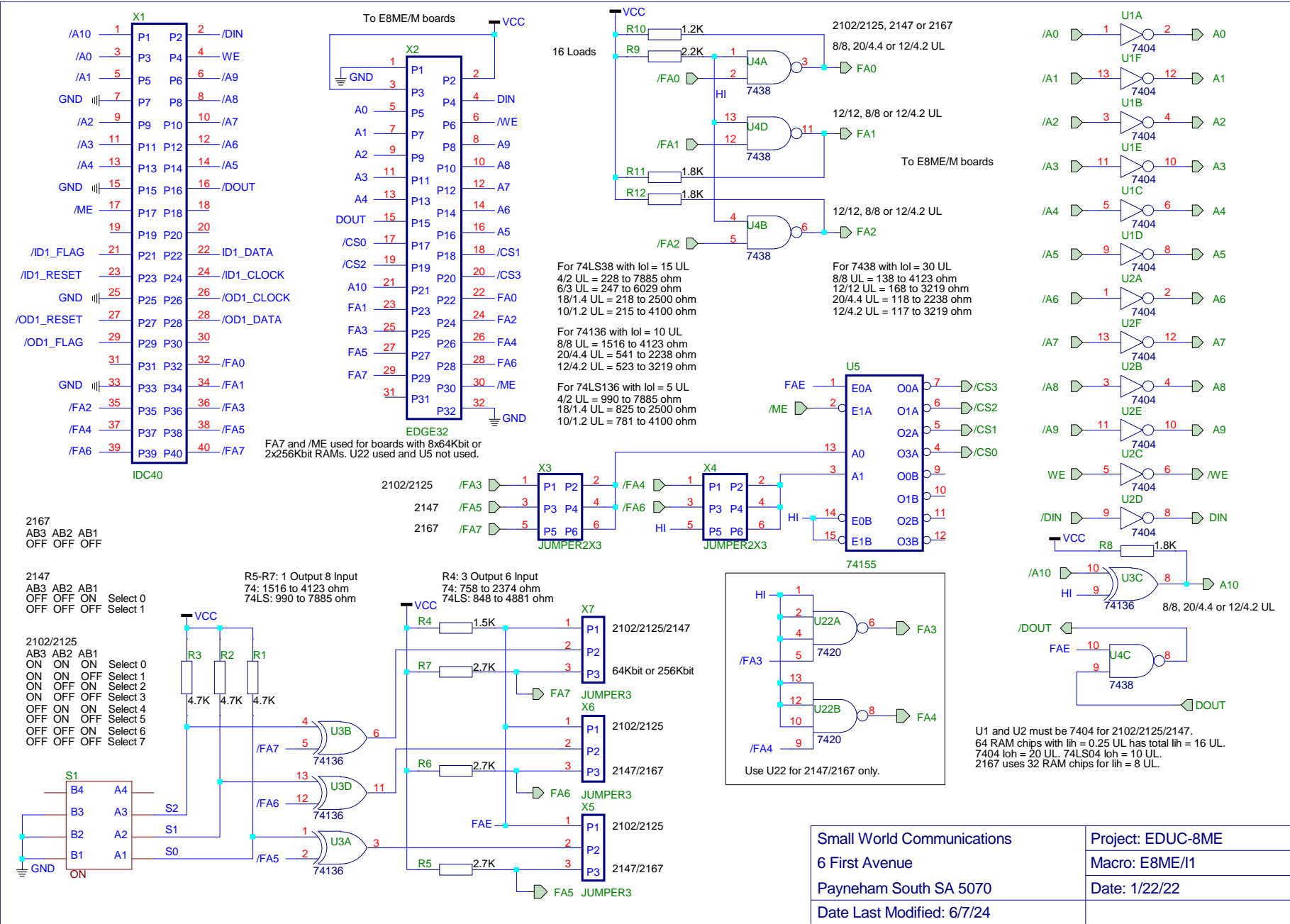
/EXT_LFA goes to /EXT_LA of front panel of first EDUC-8ME unit.
 Have R = 10 K, C = 100 nF and RC = 1 ms.
 For 74 with 1 output and 3 inputs: 433 to 6351 ohms
 For 74LS with 1 output and 3 inputs: 699 to 12812 ohms
 Choose R = 3.3K and C = 330 nF. RC = 1.089 ms.

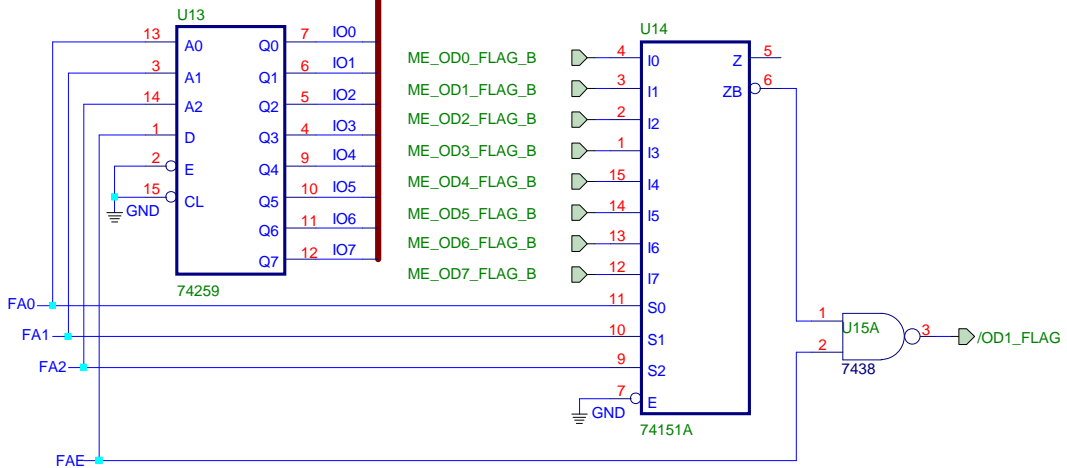
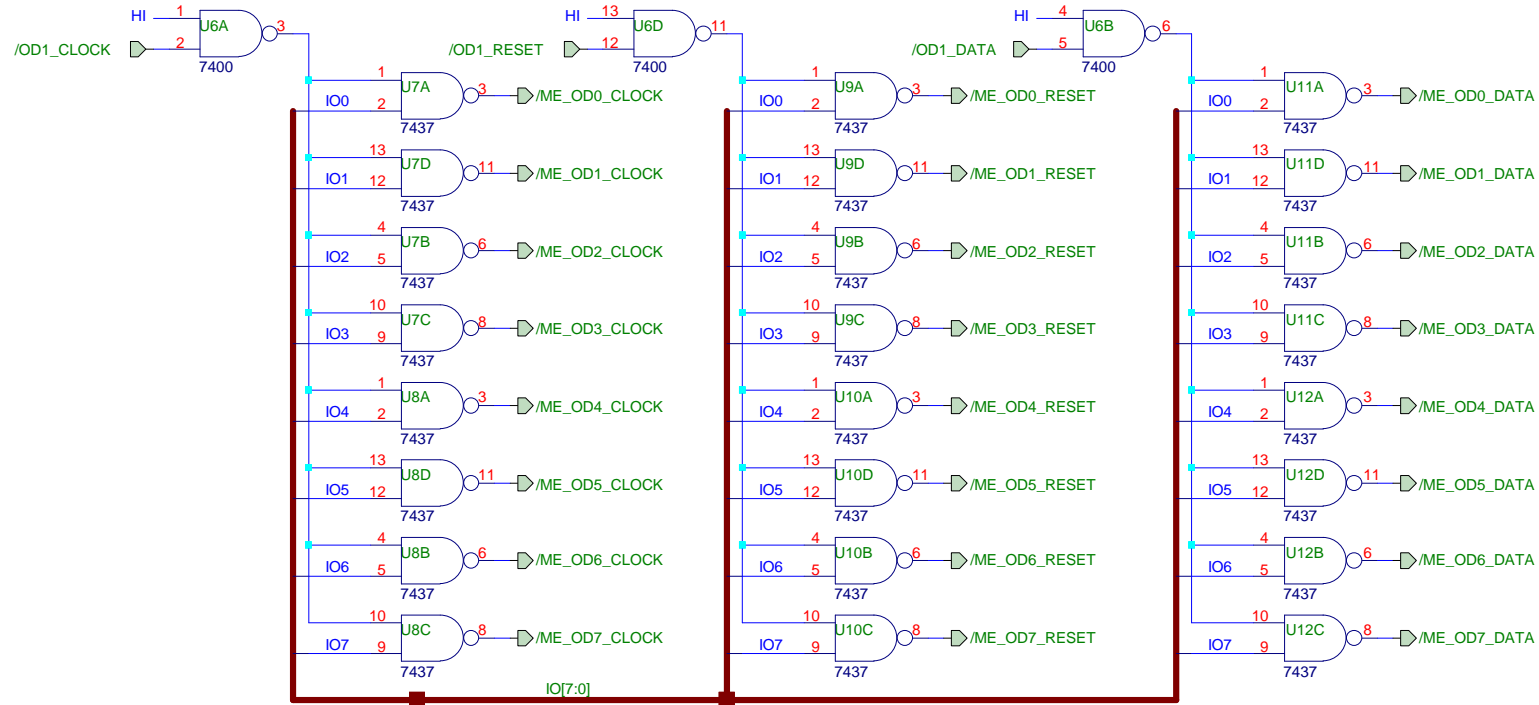
For 74LS optionally use

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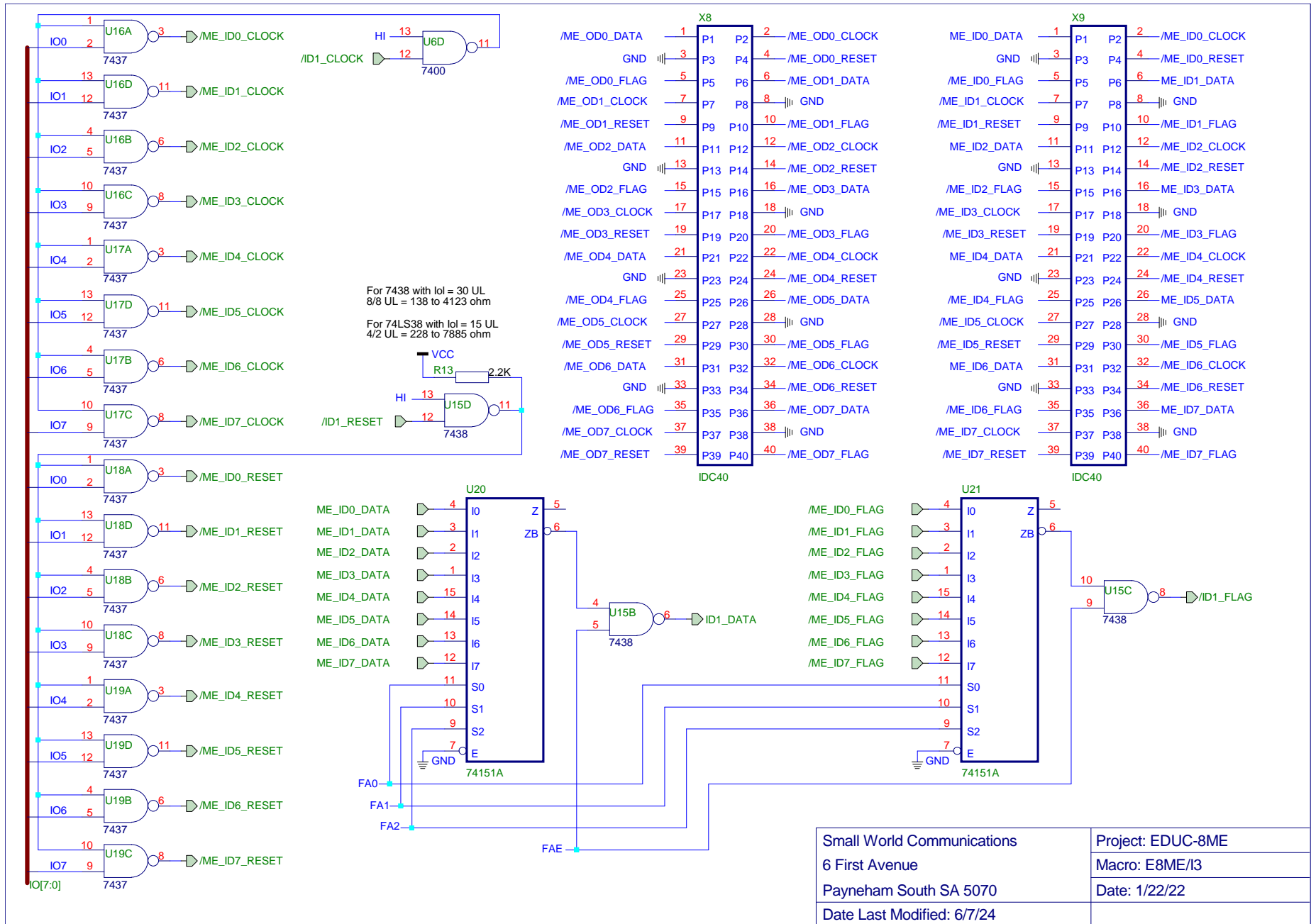


If not using MUX do not use R13, U6 to U21, X8 and X9.

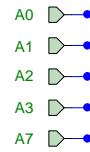
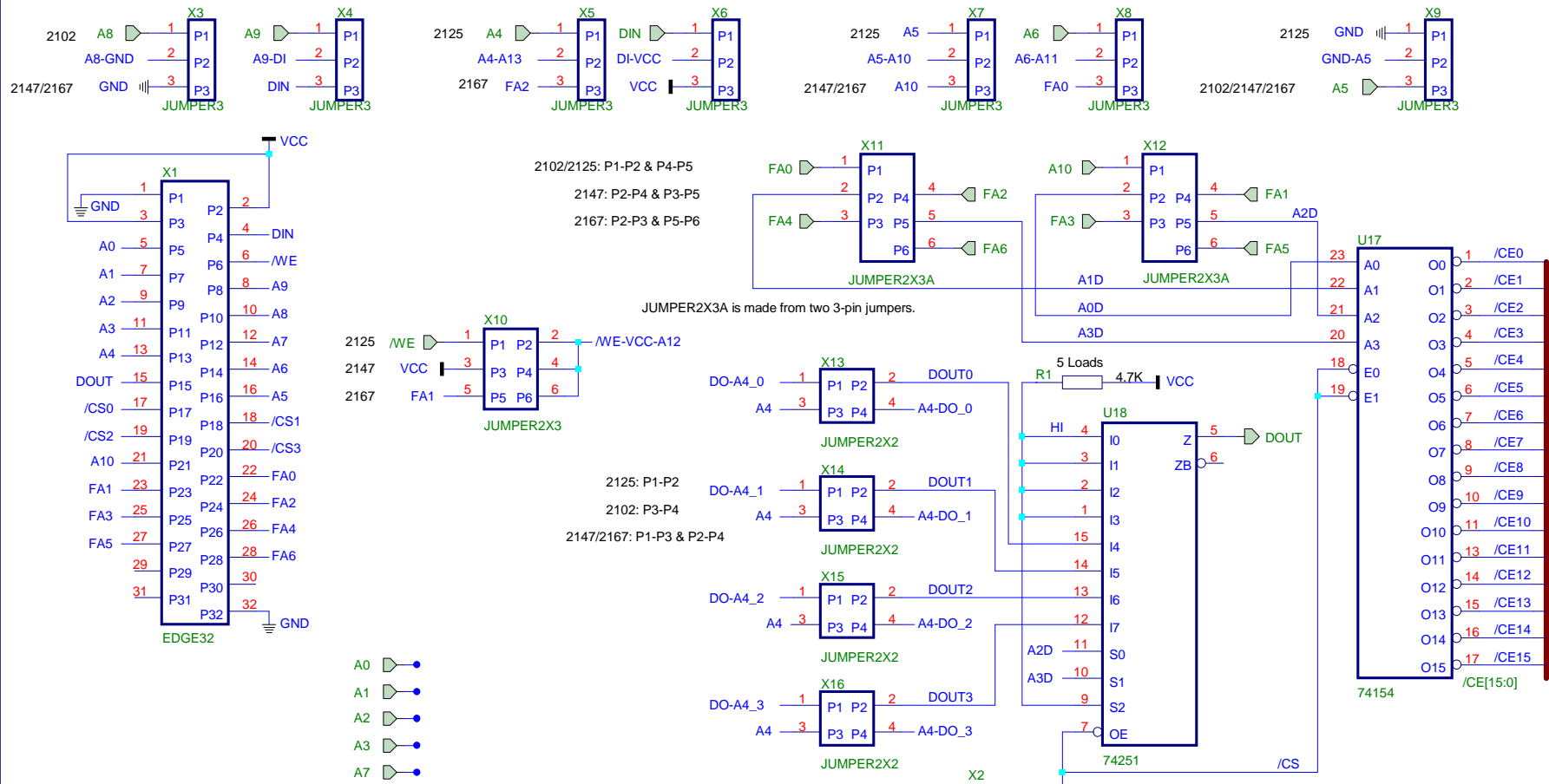
Parts List

- 1 7400 quad 2-input NAND
 - 2 7404 hex inverters
 - 1 7420 dual 4-input NAND (2147/2167 only)
 - 10 7437 quad 2-input NAND buffer
 - 2 7438 quad 2-input NAND buffer OC
 - 1 74136 quad 2-input XOR OC
 - 3 74151A 8-input multiplexer
 - 1 74155 dual 1-of-4 decoder
 - 1 74259 8-bit addressable latch
- For 74LS optionally use
- 1 1.2K resistor
 - 1 1.5K resistor
 - 3 1.8K resistors
 - 2 2.2K resistors
 - 3 2.7K resistors
 - 3 4.7K resistors
- R1/R2/R3 = 10K
 - R4 = 2.7K
 - R5/R6/R7 = 4.7K
 - R8 = 2.7K
 - R9 = 0R
 - R10 = 1.5K
 - R11/R12 = 2.2K
 - R13 = 3.9K
- 3 3-input jumpers
 - 2 2x3 jumpers
 - 1 32-way edge connector
 - 3 40-way IDC connectors

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Parts List

- 16 2102 1Kx1, 2125 1Kx1, 2147 4Kx1 or 2167 16Kx1 static RAMs
- 1 74154 1 of 16 decoder
- 1 74251 8-input multiplexer 3S
- 1 4.7K resistor
- 4 2x2 jumpers
- 1 2x3 jumper
- 1 2x4 jumper
- 11 3-pin jumpers
- 1 32-way edge connector

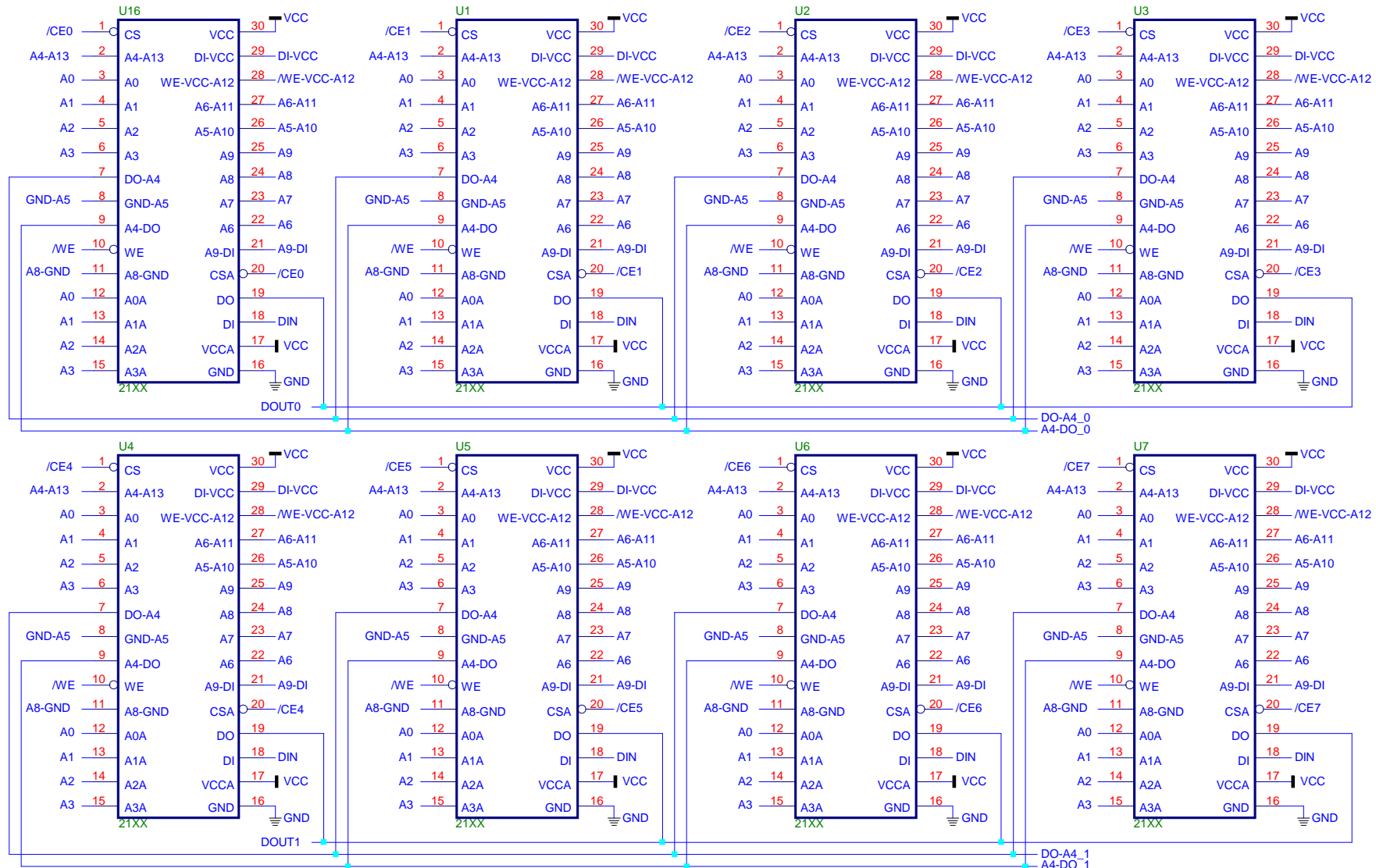
For 74LS optionally use
R1 = 0R

Layout 74154 as 4x12 pin pattern with 0.15", 0.3" and 0.15" spacing between vertical pins with left two and right two vertical pins connected horizontally. This allows 0.6" wide 74154 or 0.3" 74HCT154 to be used.

2102 has
V_{OL} = 0.45 V for I_{OL} = 1.9 mA, with I_L = -0.1 mA.
V_{OH} = 2.2 V for I_{OH} = -100 uA with I_L = 10 uA.
Thus four 2102 outputs driving one TTL input has
I_L = -1.6·3·0.1 = -1.9 mA and I_H = 40+3·10 = 70 uA.

Connect one jumper for board selection.

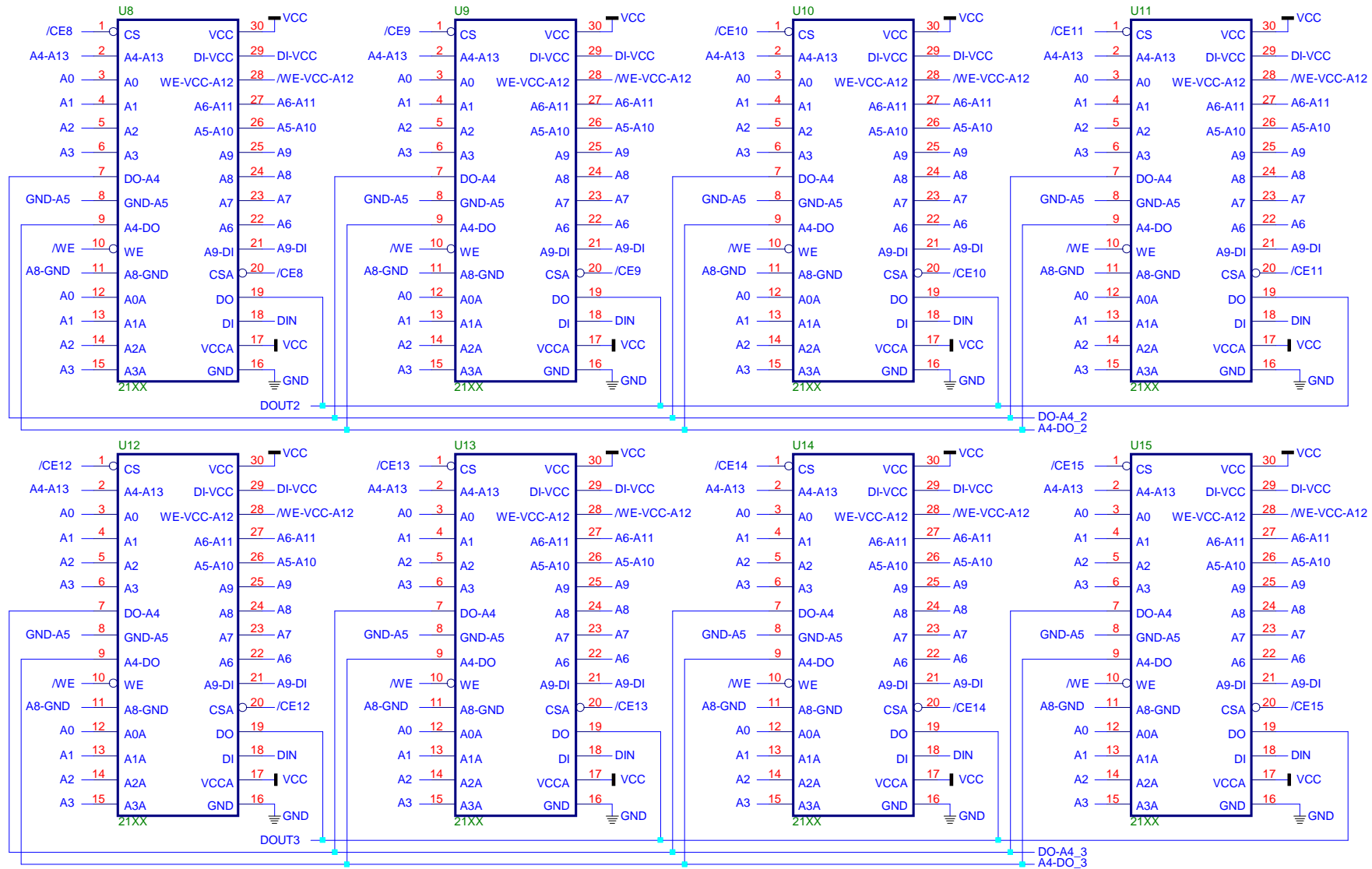
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2102 1Kx1 SRAM. Fit 16-pin DIP to pins (8-15) & (23-16)
 2125 1Kx1 SRAM. Fit 16-pin DIP to pins (1-8) & (30-23)
 2147 4Kx1 SRAM. Fit 18-pin DIP to pins (3-11) & (28-20)
 2167 16Kx1 SRAM. Fit 20-pin DIP to pins (2-11) & (29-20)

2125 compatible with TTL 93425 and CMOS 6508.

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