Small World Communications

PCE04I Inmarsat Turbo Encoder

2 November 2014 (Version 1.00) Product Specification

PCE04I Features

- 16 state Inmarsat compatible turbo encoder
- Rate 1/2 to 1/5
- Data lengths from 8 to 32,764 bits
- Up to 484 MHz internal clock
- Up to 242 Mbit/s encoding speed
- Parallel encoded data out
- 127 LUTs for Virtex–5, Virtex–6, Spartan–6 and 7–Series.
- Available as EDIF core and VHDL simulation core for Xilinx Virtex–II, Spartan–3, Virtex–4, Virtex–5, Virtex–6, Spartan–6 and 7–Series FPGAs under SignOnce IP License. Actel, Altera and Lattice FPGA cores available on request.
- Available as VHDL core for ASICs

Introduction

The PCE04I is a 16 state Inmarsat [1,2] compatible turbo encoder. Data lengths from 8 to 32,764 bits can be implemented. Turbo code rates from 1/2 to 1/5 can be selected. The sequential data is terminated with a tail. The data and this tail are interleaved. The input data block size is K. The interleaver size is K+4. The number of coded bits is $n(K+4)$ where the nominal code rate is $1/n$.

Figure 1 shows the schematic symbol for the PCE04I encoder. The EDIF core can be used with Xilinx Integrated Software Environment (ISE) software to implement the core in Xilinx FPGA's. The VHDL core can be used in ASIC designs.

Table 1 shows the performance achieved for various Xilinx parts. T_{cp} is the minimum clock period over recommended operating conditions. These performance figures may change due to device utilisation and configuration.

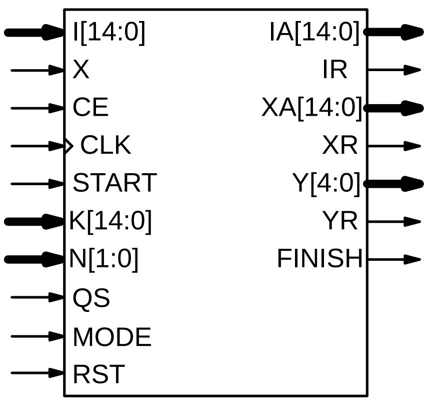

Figure 1: PCE04I schematic symbol.

Table 1: Example performance

Part	T_{cp} (ns)	Speed (Mbit/s)	
		QS = 0	**QS = 1**
XC6SLX4–2	4.493	74.2	111.3
XC6SLX4–3	3.899	85.5	128.2
XC5VLX30–1	3.296	101.1	151.7
XC5VLX30–2	2.821	118.2	177.2
XC5VLX30–3	2.503	133.2	199.8
XC6VLX75T–1	2.692	123.8	185.7
XC6VLX75T–2	2.331	143.0	214.5
XC6VLX75T–3	2.065	161.4	242.1
XC7A100T–1	4.025	82.8	124.2
XC7A100T–2	3.291	101.3	151.9
XC7A100T–3	2.919	114.2	171.3
XC7K70T–1	2.805	118.8	178.3
XC7K70T–2	2.271	146.8	220.2
XC7K70T–3	2.110	158.0	237.0
XC7Z010–1	4.014	83.0	124.6
XC7Z010–2	3.255	102.4	153.6
XC7Z010–3	2.879	115.8	173.7

Signal Descriptions

CE	Clock Enable
CLK	Encoder Clock
FINISH	Encoder Finish
I	Interleaver Address Input
IA	Interleaver Address ROM Address
IR	Interleaver Address ROM Ready
K	Data Length (8 to 32,764)
MODE	0 = small interleaver (XA[14:13] = 0)
	1 = large interleaver
N	2 = Rate 1/2
	3 = Rate 1/3
	0 = Rate 1/4
	1 = Rate 1/5
QS	Second Parity Select
	0 = Second encoded output is X, P and Q
	1 = Second encoded output is Q
RST	Synchronous Reset

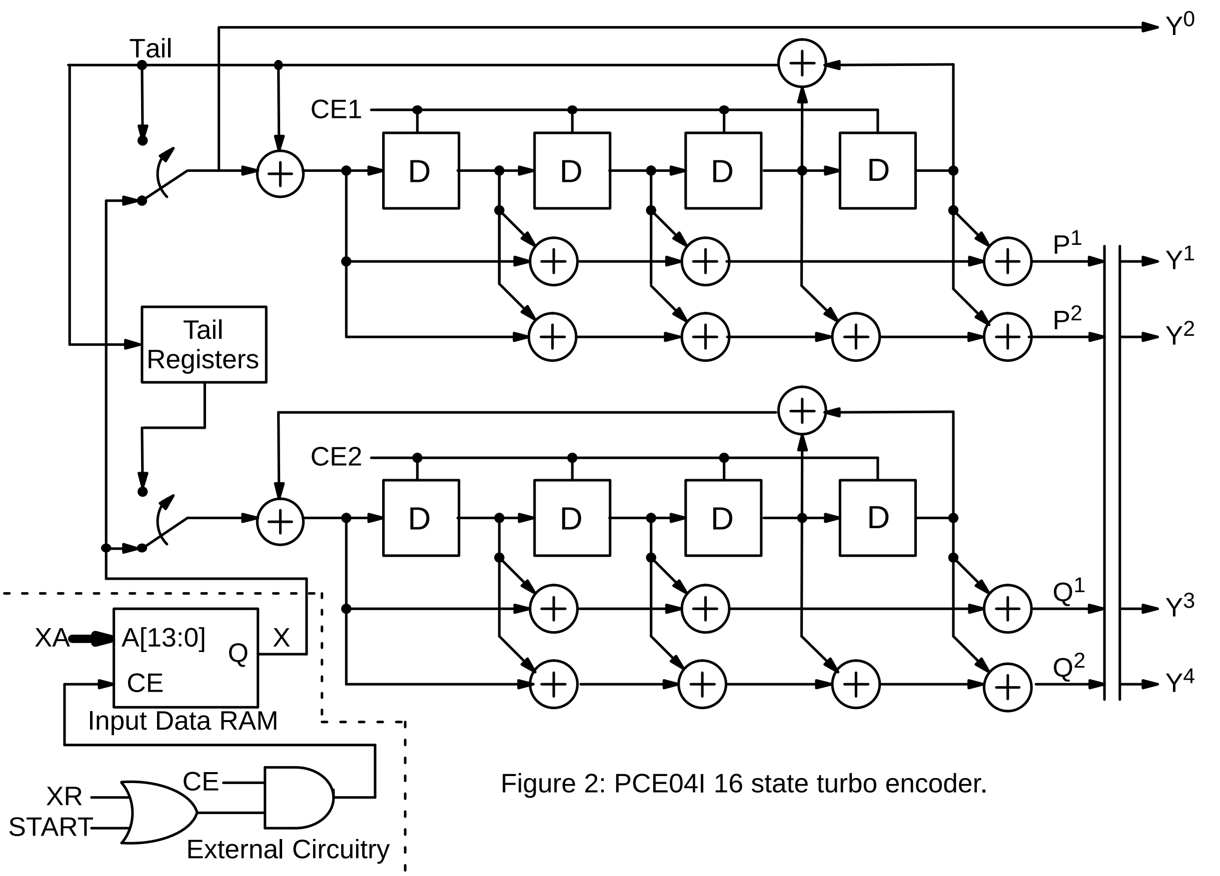

Figure 2: PCE04I 16 state turbo encoder.

START	Encoder Start
X	Data In
XA	Data In Address
XR	Data In Ready
Y	Data Out
YR	Data Out Read

Encoder

Figure 2 gives a block diagram of the PCE04I Inmarsat 16 state turbo encoder. X is the data input and Y0 to Y4 are the coded outputs. Data is clocked during the low to high transition of CLK. Separate internal clock enables (CE1 and CE2) are used to clock the data into each encoder. Non–interleaved data is clocked into the first encoder and interleaved data is clocked into the second encoder. The vertical lines indicate multiplexers

The data is first input in the sequence X_k where X_k is the data at time k from 0 to K–1. The encoder then forms the tail bits X_k from $k = K$ to K–3 which are stored in the Tail Registers. Encoded data is also output, with $Y_k^0 = X_k$, $Y_k^1 = P_k^1$ and $Y_k^2 = P_k^2$, regardless of the value of N[1:0].

If QS = 0, the data is then input in the sequence $X_k\ X_{I(k)}$ from k = 0 to K–3 where $I(k)$ is the interleaved address. Table 2 shows the output sequence for the various code rates. For rate 1/3 and 1/5, k is incremented by one from 0 to K–3. For rate 1/2 and 1/4, k is incremented by two.

If QS = 1, the data is then input in the interleaved sequence $X_{I(k)}$ from k = 0 to K–3. The encoded output is $Y_k^0 = X_{I(k)}$, $Y_k^1 = Q_k^1$ and $Y_k^2 = Q_k^2$, regardless of the value of N[1:0].

Table 2: Output sequence (QS = 0)

Rate	Sequence
1/2	$Y^0 = X_k\ X_{k+1}$
	$Y^1 = P_k^1\ Q_{k+1}^1$
1/3	$Y^0 = X_k$
	$Y^1 = P_k^1$
	$Y^2 = Q_k^1$
1/4	$Y^0 = X_k\ X_{k+1}$
	$Y^1 = P_k^1\ P_{k+1}^1$
	$Y^2 = P_k^2\ Q_{k+1}^1$
	$Y^3 = Q_k^2\ Q_{k+1}^2$
1/5	$Y^0 = X_k$
	$Y^1 = P_k^1$
	$Y^2 = P_k^2$
	$Y^3 = Q_k^1$
	$Y^4 = Q_k^2$

Figure 3 shows the initial timing diagram for encoding a block of data of length K = 1232. The encoder starts and ends in state 0. When the encod-

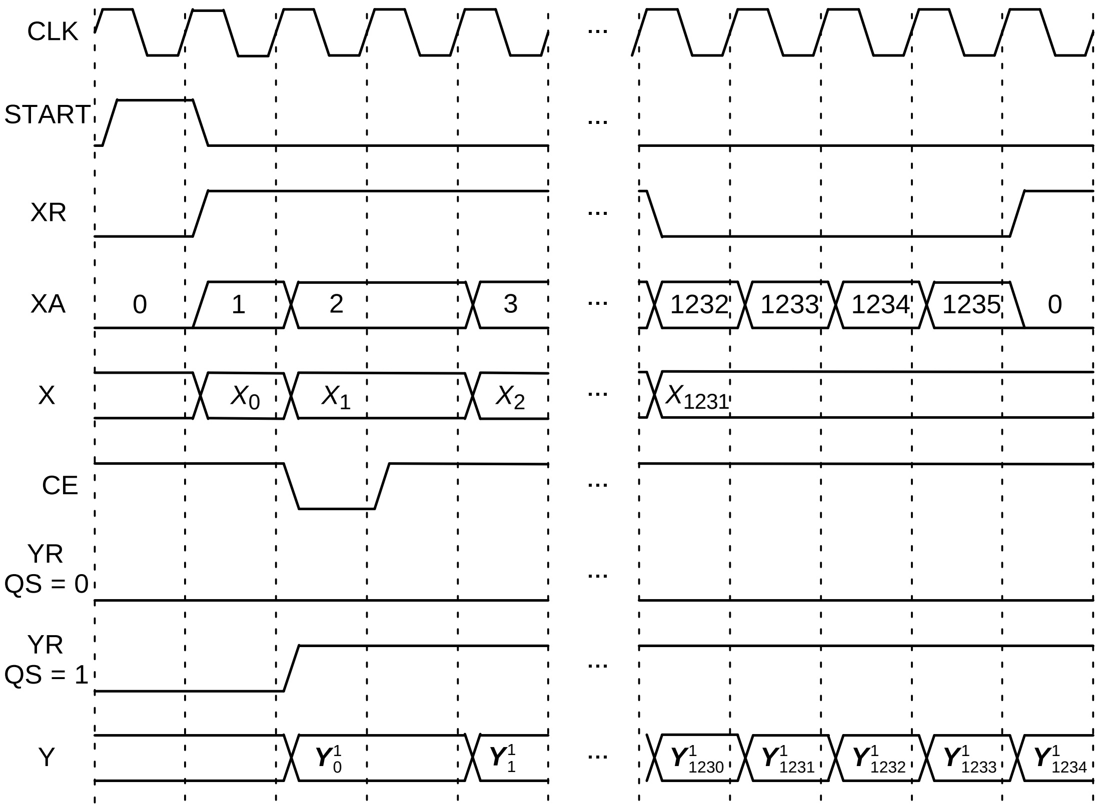

Figure 3: PCE04I Initial Encoder Timing (K = 1232).

er requires data X to be read from the input RAM, the data ready signal XR goes high (except for the first symbol) and XA[14:0] selects the data bit.

After a START signal is initiated XR goes high after one clock cycle. All signals are held if CE goes low. It is assumed that the data is stored in a synchronous read RAM with (START OR XR) AND CE used to control the read enable input of the RAM. An asynchronous read RAM can also be used by registering the RAM output. For QS = 1, the encoded data ready signal YR goes high two clock cycles after a START signal is initiated. YR is high for both the data block and tail. For QS = 0, YR stays low until the second encoded output.

Figures 4 and 5 shows the second block encoding for QS = 0 and 1, respectively. Symbol $\boldsymbol{Y}_k^1$ represents outputs with $Y_k^0 = X_k$, $Y_k^1 = P_k^1$ and $Y_k^2 = P_k^2$. Symbol $\boldsymbol{Y}_k^2$ represents outputs with $Y_k^0 = X_{I(k)}$, $Y_k^1 = Q_k^1$ and $Y_k^2 = Q_k^2$,. Symbol $\boldsymbol{Y}_k$ represents the outputs given in Table 2.

For QS = 0, the nominal encoder speed f_e is

$$f_e = \frac{f_E}{3 + 15/K} \qquad (1)$$

where $f_E = 1/T_{cp}$ is the encoder clock speed. For QS = 1 the encoder speed is

$$f_e = \frac{f_E}{2 + 8/K}. \qquad (2)$$

Ordering Information

SW–PCE04I–SOS (SignOnce Site License)
SW–PCE04I–SOP (SignOnce Project License)
SW–PCE04I–VHD (VHDL ASIC License)

All licenses include Xilinx EDIF and VHDL simulation cores. The Xilinx VHDL simulation core can only be used for simulation in the SignOnce licenses. The SignOnce Project (SOP) license allows unlimited instantiations for a specified project. The Sign–Once Site (SOS) license allows unlimited instantiations and projects for a specified development site.

Note that *Small World Communications* only provides software and does not provide the actual devices themselves. Please contact *Small World Communications* for a quote.

References

[1] University of South Australia, “Reduced bandwidth study of the High Speed Data Service Final Report,” SCRC96–6532–D005, Sep. 1996.

[2] Xu Youyun, Luo Hanwen, Song Wentao, “Application of TC in the Inmarsat mobile satellite communication systems,” Mobile Communication, 1999, 3rd.

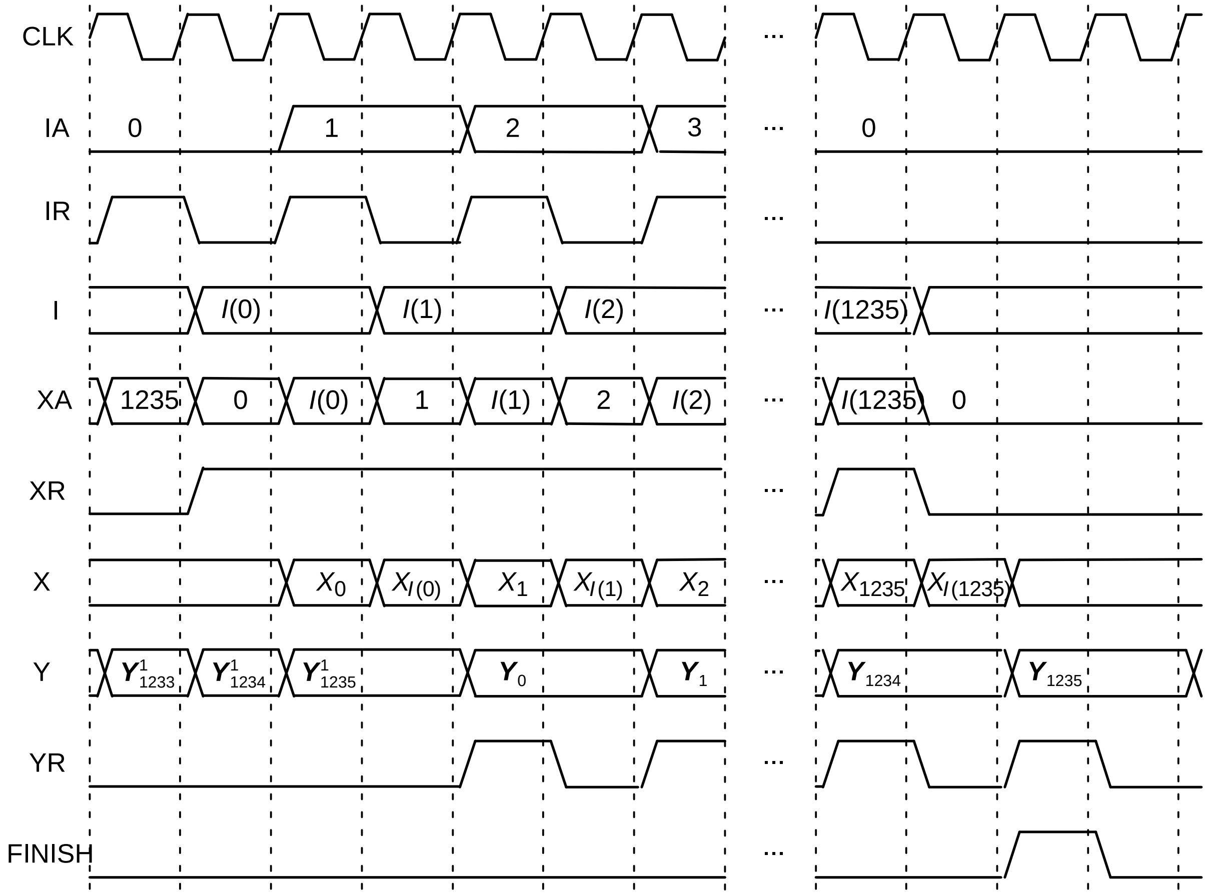

Figure 4: PCE04I Second Encoder Timing (K = 1232, QS = 0, CE = 1).

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Version History

- 0.00 28 September 2014. Preliminary product specification.
- 0.01 3 October 2014. Corrected schematic symbol and encoder diagram.
- 1.00 2 November 2014. Added LUT complexity and example performance values. Added FINISH output to encoder symbol and timing diagrams. Corrected Table 2.

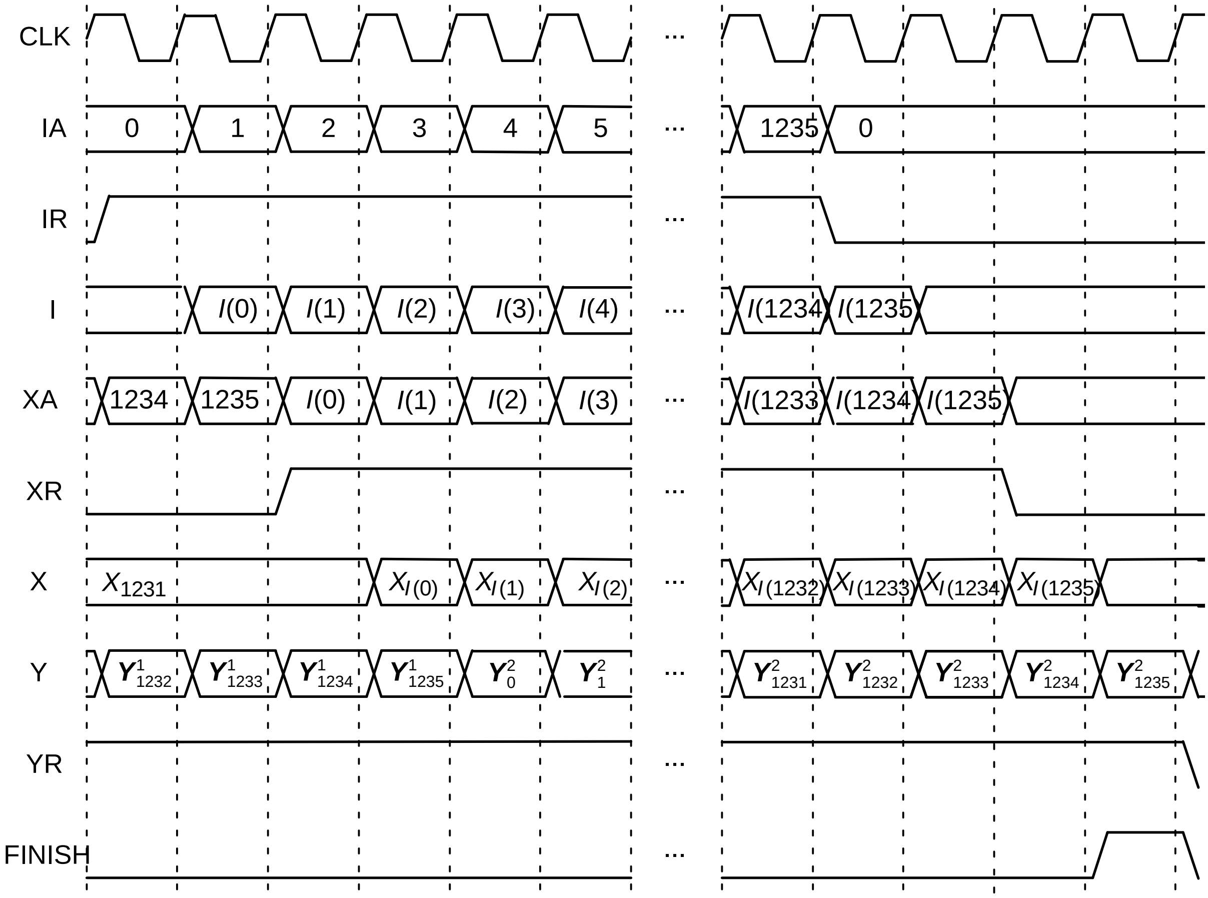

Figure 5: PCE04I Second Encoder Timing (K = 1232, QS = 1, CE = 1).