PCE04D Features

- 16 state DVB–RCS2 compatible
- Rate 1/3, 2/5, 1/2, 2/3, 3/4, 4/5, 5/6, 6/7, 7/8 with reverse output option
- Automatic puncturing
- 48 to 2048 or 5120 bit data length
- Up to 344 Mbit/s encoding speed
- 2–bit or 6–bit parallel encoded data out
- DVB–RCS2 or optional interleaver parameters
- 365 6–input LUTs
- Available as VHDL core for Xilinx FPGAs under SignOnce IP License. Intel (Altera), Lattice and Microsemi (Actel) FPGA or ASIC cores available on request.

Introduction

The PCE04D is a 16 state DVB–RCS2 [1] compatible turbo encoder. Encoded data is output 2–bits or 6–bits in parallel for increased speed. Optional external interleaver parameters can be used. The turbo code uses a 16 state rate 2/4 systematic recursive convolutional tail–biting constituent code. Since a tail–biting code is used, there are no tail bits, increasing the bandwidth efficiency of the code.

For DVB–RCS2, there are 24 interleaver sizes ranging from 112 to 4792 bits. Five parameters P, Q_0, Q_1, Q_2, and Q_3 are used by the interleaver. The decoder uses a simplified version of the interleaver with four parameters, P0I to P3I.

Figure 1 shows the schematic symbol for the PCE04D encoder. The VHDL core can be used with Xilinx Integrated Software Environment (ISE) or Vivado software to implement the core in Xilinx FPGA's.

Table 1 shows the performance achieved with 6–bit or 2–bit forward output, rate 1/2 and K = 4792 and 2–bit reverse output, rate 1/3 and K = 1504 for various Xilinx parts. T_{cp} is the minimum clock period over recommended operating conditions. These performance figures may change due to device utilisation and configuration.

The MODE input can be used to select various encoder implementations. Only one global clock is used. No other resources are used except for the external input memory.

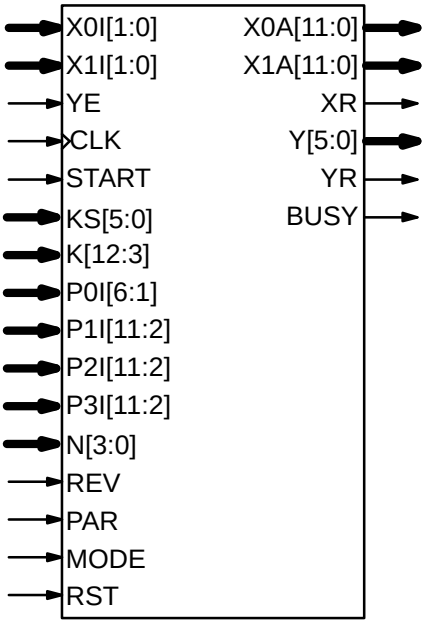

Figure 1: PCE04D schematic symbol.

Table 1: Example performance

Part	T_{cp} (ns)	Speed[1] (Mbit/s)	Speed[2] (Mbit/s)
XC7Z010–1	5.857	170.6	85.2
XC7Z010–2	4.773	209.3	104.6
XC7Z010–3	4.226	236.4	118.1
XC7A35T–1	5.852	170.7	85.3
XC7A35T–2	4.774	209.3	104.6
XC7A35T–3	4.229	236.3	118.1
XC7K70T–1	4.005	249.5	124.7
XC7K70T–2	3.159	316.3	158.1
XC7K70T–3	2.898	344.8	172.3

[1] Rate = 1/2, K = 4792, 6–bit or 2–bit forward
[2] Rate = 1/3, K = 1504, 2–bit reverse

Signal Descriptions

BUSY Encoder busy
CLK Clock
K Data Length (48 to 2048 with MODE = 0 or 48 to 5120 with MODE = 1)
K[12:3] = K/8
KS KS Data Length Select
0 = select K, P0I–P3I

1,3 = length 304 (38 bytes)
2 = length 112 (14 bytes)
4 = length 472 (59 bytes)
5 = length 680 (85 bytes)
6 = length 768 (96 bytes)
7 = length 864 (108 bytes)
8 = length 920 (115 bytes)
9 = length 1040 (130 bytes)
10 = length 1152 (144 bytes)
11 = length 1400 (175 bytes)
12 = length 1552 (194 bytes)
13 = length 984 (123 bytes)
14 = length 1504 (188 bytes)
15 = length 2112 (264 bytes)
16 = length 2384 (298 bytes)
17 = length 2664 (333 bytes)
18 = length 2840 (355 bytes)
19 = length 3200 (400 bytes)
20 = length 3552 (444 bytes)
21 = length 4312 (539 bytes)
22 = length 4792 (599 bytes)
32,33 = length 800 (100 bytes)
34–36 = length 1360 (170 bytes)
37–39 = length 3504 (438 bytes)

MODE Mode select
0 = 1K Interleaver
1 = 2.5K Interleaver (DVB–RCS2)

N Code Rate (see page 3 for notation)
0 = rate 1/2 ($\mathbf{p}_2 = 1$, $\mathbf{p}_3 = 0$)
1 = rate 2/3 ($p_2 = 2$, $\mathbf{q}_2 = (0)$, $\mathbf{p}_3 = 0$)
2 = rate 3/4 ($p_2 = 6$, $\mathbf{q}_2 = (0,2)$, $\mathbf{p}_3 = 0$)
3 = rate 4/5 ($p_2 = 4$, $\mathbf{q}_2 = (0)$, $\mathbf{p}_3 = 0$)
4 = rate 5/6 ($p_2 = 20$, $\mathbf{q}_2 = (0,4,8,12)$, $\mathbf{p}_3 = 0$)
5 = rate 6/7 ($p_2 = 12$, $\mathbf{q}_2 = (0,4)$, $\mathbf{p}_3 = 0$)
6 = rate 7/8 ($p_2 = 28$, $\mathbf{q}_2 = (0,4,12,20)$, $\mathbf{p}_3 = 0$)
8 = rate 1/3 ($\mathbf{p}_2 = 1$, $\mathbf{p}_3 = 1$)
9 = rate 2/5 ($\mathbf{p}_2 = 1$, $\mathbf{p}_3 = 10$)

P0I–P3I Interleaver parameters (used when KS = 0).
P0I[6:1] = P div 2
P1I[11:2] = Q_1
P2I[11:2] = $(Q_0P + Q_2) \bmod K/8$
P3I[11:2] = $(Q_0P + Q_3) \bmod K/8$

PAR Parallel Encoded Data Select
0 = 2–bit
1 = 6–bit

REV Reverse data output
0 = Input data output first
1 = Input data output last

RST Synchronous Reset
START Encoder Start
X0I Non–interleaved Data In
X1I Interleaved Data In
X0A Non–interleaved Data In Address
X1A Interleaved Data In Address
XR Data In Ready
Y Encoded Data Out (data and parity)
YE Encoded Data Out Enable
YR Data Out Ready

Note that MODE is a “soft” input and should not be connected to input pins or logic. This input is designed to minimise decoder complexity for the configuration selected.

Encoder

Figure 2 gives a block diagram of the PCE04D DVB–RCS2 16 state turbo encoder. X0I[1:0] and X1I[1:0] are the data and interleaved data input, respectively and Y[1:0] (PAR = 0) or Y[5:0] (PAR = 1) are the coded outputs. Data is clocked during the low to high transition of CLK. In the first $K/2$ clock cycles, data is input to the encoders starting from state 0. The final state of this sequence along with the value of $K/2$ mod 15, determines the tail–biting state T[3:0] which is selected by TS. Note that if $K/2$ is divisible by 15 ($K/2$ mod 15 = 0) then tail–biting is not possible for all input sequences. In the following $K/2$ to $3K/2$ clock cycles, encoded data is produced. For punctured codes, parity data is stored in the RAM so that it can then be sequentially read out.

Let $\boldsymbol{X}_k = \left\{X_k^0, X_k^1\right\} = \left\{Y_{0,k}^0, Y_{0,k}^1\right\} = \{A_k, B_k\} =$ {X0I[0],X0I[1]} be the input data to X0I[1:0] at time k, from 0 to K–1. The input data to X1I[1:0] is $\boldsymbol{X}_{I(k)} = \left\{X_{I(k)}^0, X_{I(k)}^1\right\} = \left\{Y_{1,k}^{\overline{f(k)}}, Y_{1,k}^{f(k)}\right\} = \left\{A_{I(k)}, B_{I(k)}\right\}$ where $I(k)$ is the interleaved address and $f(k) = k \bmod 2$. The term $Y_{j,k}^i$ refers to the coded output at time k, i is the index of the coded bit ($0 \le i \le 3$) and j indicates whether the coded sequence corresponds to an interleaved input of $\boldsymbol{X}_k$, i.e., if $j = 0$ the input data is $\boldsymbol{X}_k$ and if $j = 1$ the input data is $\boldsymbol{X}_{I(k)}$. The terms $\{A_k, B_k\}$ corresponds to the notation used in the standard.

Let $\boldsymbol{Y}_k^2 = \left\{Y_{0,k}^2, Y_{1,k}^2\right\} = \left\{Y_{1,k}, Y_{2,k}\right\}$ and $\boldsymbol{Y}_k^3 = \left\{Y_{0,k}^3, Y_{1,k}^3\right\} = \left\{W_{1,k}, W_{2,k}\right\}$ be the first and second coded parity bits, respectively, each corresponding to non–interleaved and interleaved input data. The terms $\left\{Y_{1,k}, Y_{2,k}\right\}$ and $\left\{W_{1,k}, W_{2,k}\right\}$ corresponds to the notation used in the standard.

Table 2 shows the 2–bit output (PAR = 0) delay and output sequence depending on the code rate and whether the reverse output mode is selected. The additional three clock cycles are due to the START input and then a two clock cycle pipeline

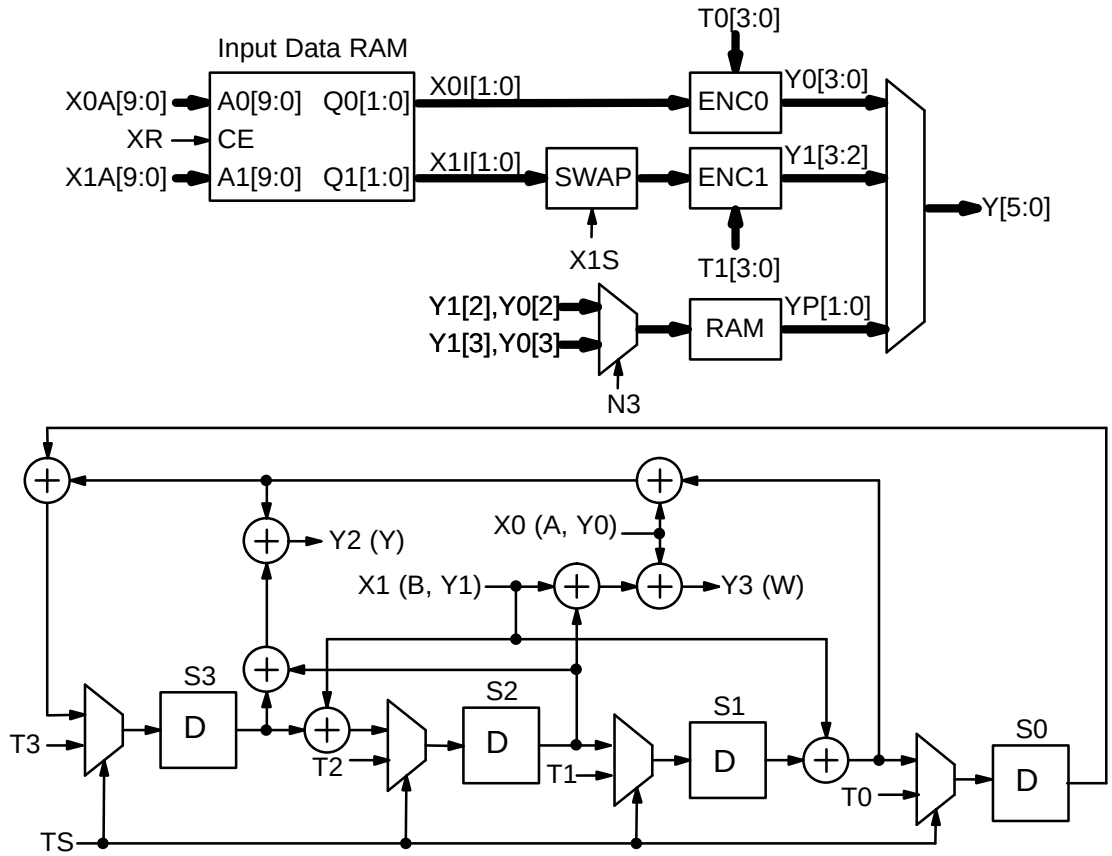

Figure 2: PCE04D DVB–RCS2 16 state turbo encoder.

delay. For 6–bit output (PAR = 1) the delay is $K/2+3$ and the encoding time is $K+3$.

Table 2: Output Sequence for 2–bit Output

REV	Rates	Delay	Sequence	Time (*T*)
0	1/2	3	$\boldsymbol{X}\,\boldsymbol{Y}^2$	$K+3$
0	2/3–7/8	$K/2+3$	$\mathbf{0}\,\boldsymbol{X}\,\boldsymbol{Y}^2$	$K+L_2+3$
0	1/3	3	$\boldsymbol{X}\,\boldsymbol{Y}^2\,\boldsymbol{Y}^3$	$1.5K+3$
0	2/5	$K/2+3$	$\mathbf{0}\,\boldsymbol{X}\,\boldsymbol{Y}^2\,\boldsymbol{Y}^3$	$1.5K+L_3+3$
1	1/2	$K/2+3$	$\mathbf{0}\,\boldsymbol{Y}^2\,\boldsymbol{X}$	$1.5K+3$
1	2/3–7/8	$K+3$	$\mathbf{0}\,\mathbf{0}\,\boldsymbol{Y}^2\,\boldsymbol{X}$	$1.5K+L_2+3$
1	1/3–2/5	$K/2+3$	$\mathbf{0}\,\boldsymbol{Y}^2\,\boldsymbol{Y}^3\,\boldsymbol{X}$	$1.5K+L_3+3$

The terms $\boldsymbol{X} = \left\{\boldsymbol{X}_0, \ldots, \boldsymbol{X}_{K/2-1}\right\}$, $\boldsymbol{Y}^2 = \{\boldsymbol{Y}^2_{f_2(j)}, 0 \le j \le L_2\text{–}1\}$, $\boldsymbol{Y}^3 = \{\boldsymbol{Y}^3_{f_3(j)}, 0 \le j \le L_3\text{–}1\}$ and $\mathbf{0} = \{\{0,0\}, 0 \le j \le K/2\text{–}1\}$ are used to describe the coded sequence outputs where $L_i, 2 \le i \le 3$ correspond to the lengths of the punctured sequences and $f_i(j)$ indicates the non–punctured bit positions. We have that

$$L_i = \left\lfloor \frac{K}{2p_i} \right\rfloor \frac{p_i}{k} + \sum_{j=0}^{K/2 \bmod p_i - 1} \mathbf{p}_i(j) \qquad (1)$$

where p_i is the puncturing period, k/n is the nominal code rate, $\mathbf{p}_i = \mathbf{p}_i(0)\ldots\mathbf{p}_i(p_i\text{–}1)$ is the puncturing vector, $\mathbf{p}_i(j)$ is 0 or 1 and $\mathbf{q}_i = (q_i(0),\ldots,q_i(p_i/k\text{–}1))$ indicates the non–punctured positions in $\mathbf{p}_i$. We can express the puncturing pattern either directly, e.g., $\mathbf{p}_2 = 1001000$ or by indicating the non–punctured positions in the vector, e.g., $\mathbf{q}_2 = (0,2)$.

For rates 1/2 to 7/8 we have $p_2 = 1, 2, 6, 4, 20, 12$ and 28, respectively ($\boldsymbol{Y}^3$ is not output so p_3 is not defined). For rates 1/3 and 2/5 we have $p_2 = 1$ and $p_3 = k$.

Table 3 shows the relation ship between the input and output bits and the notation used for PAR = 1. Note that no puncturing is performed with PAR = 1, i.e., the inputs N[3:0] are ignored.

Note that the output is in one continuous stream. The encoder does not pause (unless YE goes low) in outputting the data.

Figure 3 shows the initial timing diagram for encoding a block of data of length $K = 680$. When the encoder requires data X0I[1:0] and X1I[1:0] to be read from the input RAM, the data ready signal XR goes high and X0A[11:0] and X1A[11:0] selects the non–interleaved and interleaved data bits. After a START signal is initiated XR goes high. It is assumed that the data is stored in a synchrono-

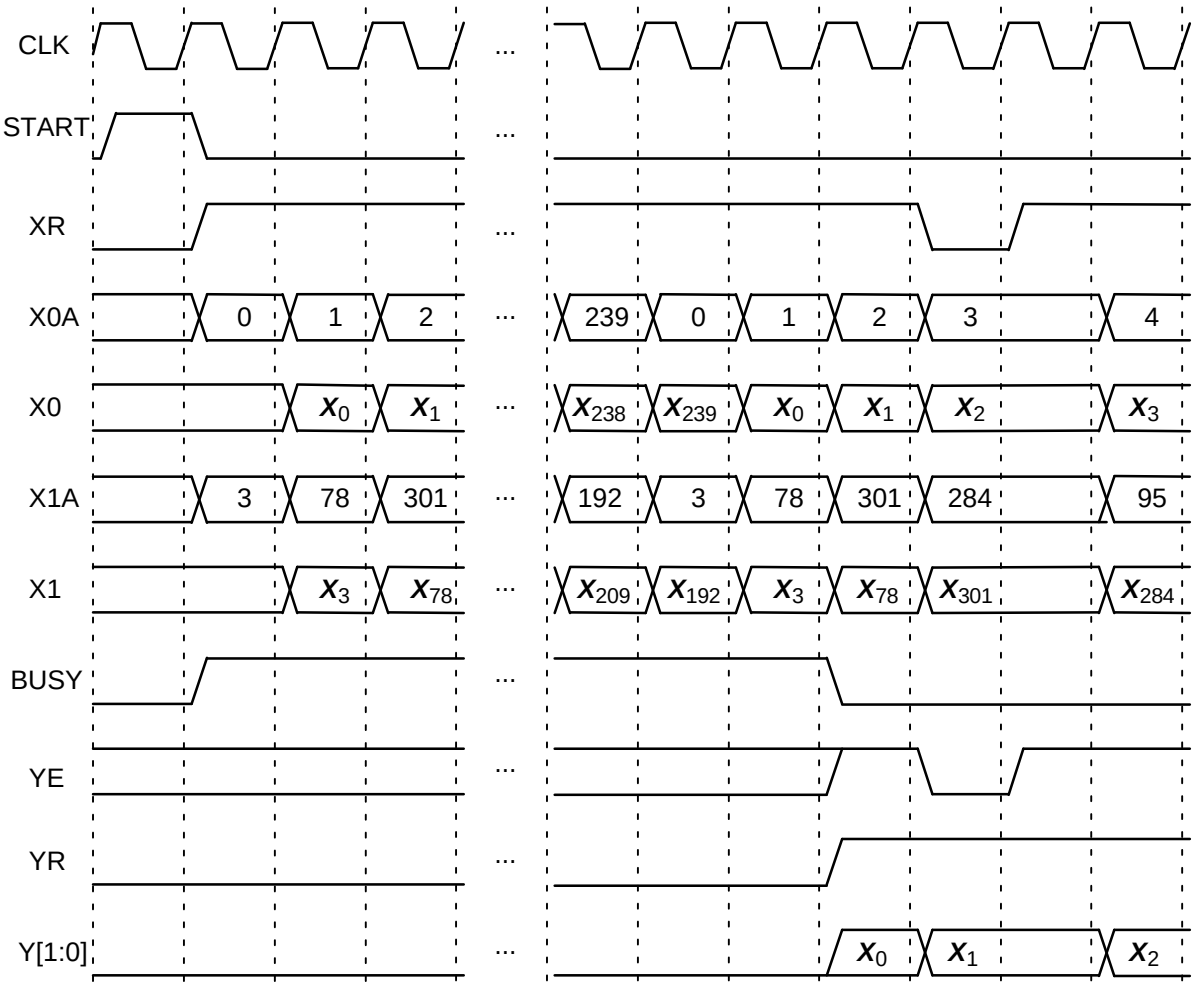

Figure 3: PCE04D Initial Encoder Timing (K = 680, R = 2/3, 2–bit DVB–RCS2).

us read dual port RAM (or two single port RAMs) with XR used to control the enable input of the RAM. An asynchronous read RAM can also be used by registering the RAM output.

Table 3: Input/Output Notation for PAR = 1

PCE04D	Standard	Uniform
X0I[0]	A_k	$X_k{}^0$
X0I[1]	B_k	$X_k{}^1$
X1I[0]	$A_{I(k)}$	$X_{I(k)}{}^0$
X1I[1]	$B_{I(k)}$	$X_{I(k)}{}^1$
Y[0]	A_k	$Y_{0,k}{}^0 = X_k{}^0$
Y[1]	B_k	$Y_{0,k}{}^1 = X_k{}^1$
Y[2]	Y_{1k}	$Y_{0,k}{}^2$
Y[3]	Y_{2k}	$Y_{1k}{}^2$
Y[4]	W_{1k}	$Y_{0,k}{}^3$
Y[5]	W_{2k}	$Y_{1k}{}^3$

The encoded data ready signal YR goes high *2, K*/2+2 or *K*+2 clock cycles after a START signal is initiated, during which time BUSY is high. If YE is low and YR is high the encoder is held during the next low–to–high transition of CLK. The output of XR also goes low when YE goes low so that the data RAM output is held. When encoding is completed YR goes low.

The nominal input data rate f_e is

$$f_e = \frac{f_E K}{T} \qquad (2)$$

where $f_E = 1/T_{cp}$ is the encoder clock speed and T is the decoding time as given in Table 2 for PAR = 0. For PAR = 1 we have $T = K+3$.

Interleaver parameters

The interleaving equation is given by

$$\pi(j) = (Pj + Q(j \bmod 4) + 3) \bmod K/2 \qquad (3)$$

where j varies from 0 to $K/2-1$. Table 4 gives the formulas for $Q(j)$.

The parameters P and Q_0 to Q_3 depend on the block length K. These values are given in the standard. P is an odd number while Q_0 to Q_3 can be odd or even numbers. To reduce interleaver complexity, we let $P(j) = Q(j) \bmod K/2$ for j = 1 to 3. We have that

Table 4: Interleaver Parameters

j	*Q(j)*
0	0
1	$4Q_1$
2	$4Q_0P + 4Q_2$
3	$4Q_0P + 4Q_3$

$$Q(j) = D(j)K/2 + P(j) \quad (4)$$

where $D(j) = Q(j)$ div $K/2$. As four divides $Q(j)$ and $K/2$, four must also divide $P(j)$. That is

$$Q(j)/4 = D(j)K/8 + P(j)/4. \quad (5)$$

Since $P(j)/4 < K/8$ the decoder uses $P_j = Q(j)/4$ mod $K/8$ for $j = 1$ to 3 for the internal parameters. The term $Q(0)$ does not need to be externally input since it is always zero. We also let $P_0 = P$ div 2.

When KS[5:0] = 0, the byte length $K/8$ is input to K[12:3] and the interleaver parameters P_0 to P_3 are input to P0I[6:1] and P1I[11:2] to P3I[11:2], respectively. Internally, the two least significant bits PjI[1:0] = 0, $1 \leq j \leq 3$, and least significant bit P0I[0] = 1.

When KS[5:0] > 0, the internal data length selected by KS (equal to the Waveform ID) is used. Also, the internal interleaver parameters P_0 to P_3 for the data length from the standard are used. The inputs K[12:3], P0I[6:1], and P1I[11:2] to P3I[11:2] are ignored.

Ordering Information

SW–PCE04D–SOS (SignOnce Site License)
SW–PCE04D–SOP (SignOnce Project License)
SW–PCE04D–VHD (VHDL ASIC License)

All licenses include Xilinx VHDL cores. The SignOnce and ASIC licenses allows unlimited instantiations and free updates for one year.

Note that *Small World Communications* only provides software and does not provide the actual devices themselves. Please contact *Small World Communications* for a quote.

References

[1] EBU–UER and DVB, “Digital video broadcasting second generation interactive satellite system (DVB–RCS2) Part 2: Lower layers for satellite standard,” ETSI EN 301 545–2 V1.1.1, Jan. 2012.

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Version History

- 1.00 19 November 2018. First release.
- 1.01 12 December 2018. Clarified definition of X0I[1:0].