PCE04C Features

- 16 state CCSDS compatible turbo encoder
- Rate 1/2 to 1/7
- Interleaver sizes from 1784 to 16056 bits
- Up to 447 MHz internal clock
- Up to 223 Mbit/s encoding speed
- Serial continuous encoded data out
- 128 LUTs for Virtex–5, Virtex–6 and 7–Series
- Available as VHDL core for Xilinx FPGAs under SignOnce IP License. ASIC, Altera, Lattice and Microsemi cores available on request.

Introduction

The PCE04C is a 16 state CCSDS [1] compatible turbo encoder. Interleaver sizes from 1784 to 16056 bits in multiples of 1784 can be implemented. Turbo code rates from 1/2 to 1/7 can be selected. The un–interleaved data is terminated with a tail using both data and parity information. The interleaved data is terminated with a tail using parity data only. The input block and interleaver size is K. The number of coded bits is $n(K+4)$ where the nominal code rate is $1/n$.

Figure 1 shows the schematic symbol for the PCE04C encoder. The VHDL core can be used with Xilinx Integrated Software Environment (ISE) or Vivado software to implement the core in Xilinx FPGA's.

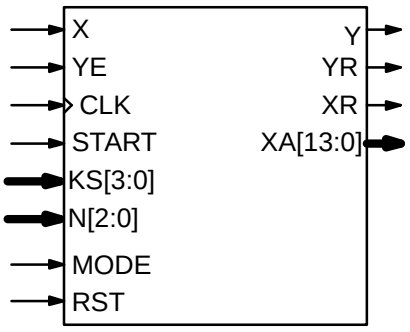

Figure 1: PCE04C schematic symbol.

Table 1 shows the performance achieved for various Xilinx parts for K = 1784. T_{cp} is the minimum clock period over recommended operating conditions. These performance figures may change due to device utilisation and configuration.

Table 1: Example performance

Part	T_{cp} (ns)	Speed (Mbit/s)			
		1/2	1/3	1/4	1/6
XC5VLX30–1	4.155	120.0	80.0	60.0	40.0
XC5VLX30–2	3.559	140.0	93.4	70.0	46.7
XC5VLX30–3	3.164	157.5	105.0	78.8	52.5
XC6VLX75T–1	3.271	152.4	101.6	76.2	50.8
XC6VLX75T–2	2.799	178.1	118.7	89.0	59.4
XC6VLX75T–3	2.483	200.8	133.8	100.4	66.9
XC7Z010–1	4.612	108.1	72.0	54.0	36.0
XC7Z010–2	3.767	132.3	88.2	66.1	44.1
XC7Z010–3	3.343	149.1	99.4	74.5	49.7
XC7A35T–1	4.515	110.4	73.6	55.2	36.8
XC7A35T–2	3.678	135.5	90.3	67.8	45.2
XC7A35T–3	3.277	152.1	101.4	76.0	50.7
XC7K70T–1	2.988	166.8	111.2	83.4	55.6
XC7K70T–2	2.413	206.6	137.7	103.3	68.9
XC7K70T–3	2.233	223.2	148.8	111.6	74.4

Signal Descriptions

CLK	Encoder Clock
KS	Interleaver Size Select (0 to 8, Block Length K = 1784(KS+1))
MODE	0 = small interleaver (XA[13:12] = 0) 1 = large interleaver
N	Code Rate (2 to 7)
RST	Synchronous Reset
START	Encoder Start
X	Data In
XA	Data In Address
XR	Data In Ready
Y	Data Out
YE	Data Out Enable
YR	Data Out Ready

Encoder

Figure 2 gives a block diagram of the PCE04C CCSDS 16 state turbo encoder. X is the data input and Y0 to Y6 are the coded outputs. Data is clocked during the low to high transition of CLK. Separate internal clock enables (CE1 and CE2) are used to clock the data into each encoder. Non–interleaved data is clocked into the first en-

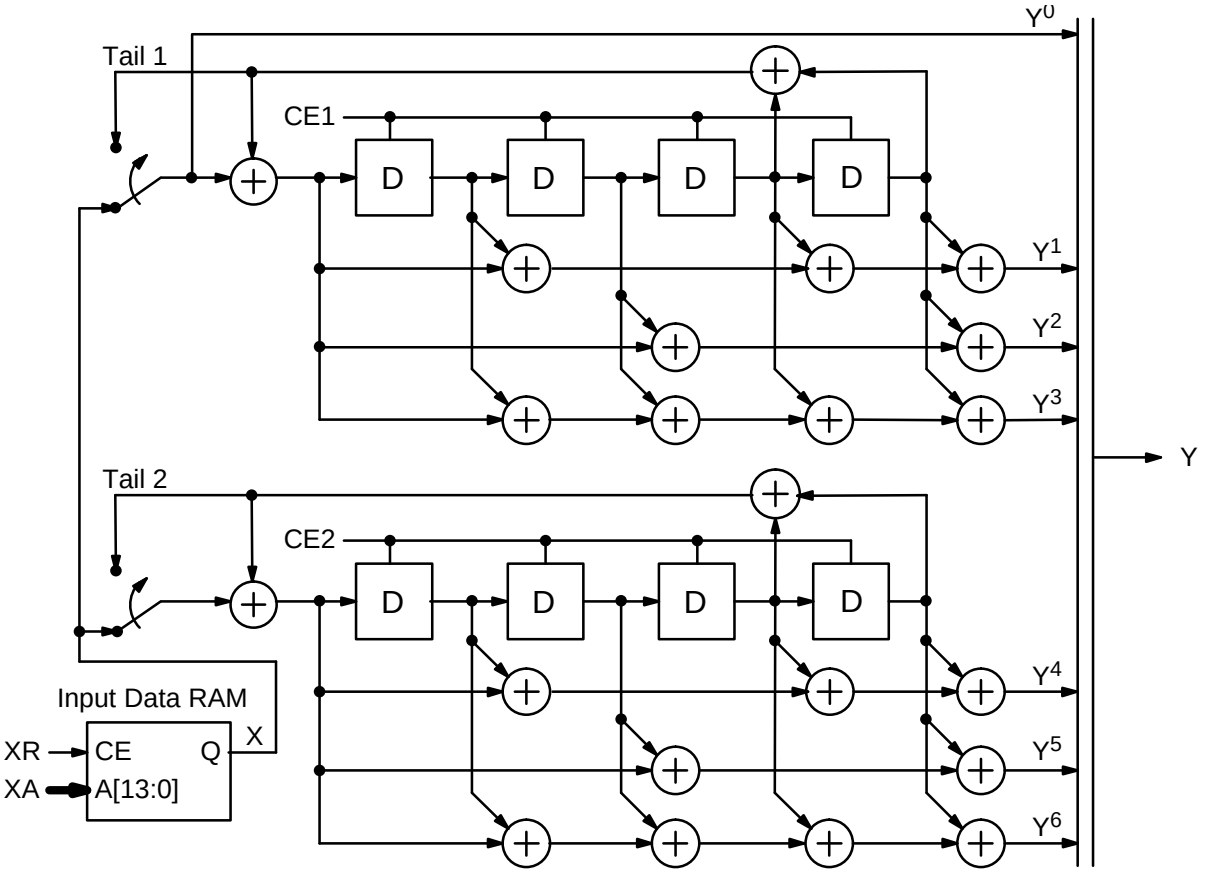

Figure 2: PCE04C 16 state turbo encoder.

coder and interleaved data is clocked into the second encoder. The twin vertical lines indicate a multiplexer.

The data is input in the sequence X_k $X_{I(k)}$ where X_k is the data at time k from 0 to K–1 and $I(k)$ is the interleaved address. Table 2 shows the output sequence for the various code rates. For rate 1/3 to 1/7, k is incremented by one from 0 to K–1. For rate 1/2, k is incremented by two.

Table 2: Output sequence

Rate	Sequence
1/2	Y_k^0 Y_k^1 Y_{k+1}^0 Y_{k+1}^4
1/3	Y_k^0 Y_k^1 Y_k^4
1/4	Y_k^0 Y_k^2 Y_k^3 Y_k^4
1/5	Y_k^0 Y_k^2 Y_k^3 Y_k^4 Y_k^5
1/6	Y_k^0 Y_k^1 Y_k^2 Y_k^3 Y_k^4 Y_k^6
1/7	Y_k^0 Y_k^1 Y_k^2 Y_k^3 Y_k^4 Y_k^5 Y_k^6

Note that the output for all rates is output in one continuous stream. The encoder does not pause (unless YE goes low) in outputting the data. The tail bits are output in the same sequence as the data sequence.

Figure 3 shows the initial timing diagram for encoding a block of data of length K = 1784 with R=1/3. The encoder starts and ends in state 0. When the encoder requires data X to be read from the input RAM, the data ready signal XR goes high and XA[13:0] selects the data bit. After a START signal is initiated XR goes high after one cycle (this occurs for all rates). It is assumed that the data is stored in a synchronous read RAM with XR used to control the enable input of the RAM. An asynchronous read RAM can also be used by registering the RAM output.

If YE is high, the encoded data ready signal YR goes high three clock cycles after a START signal is initiated (this occurs for all rates). YR is high for both the data block and tail. If YE is low the encoder is held during the next low–to–high transition of CLK. The output of XR also goes low when YE goes low so that the data RAM output is held. Figure 4 shows the encoding process for the tail with KS = 0 (K = 1784).

The nominal input data rate f_e is

$$f_e = \frac{f_E}{n + (4n + 2)/K} \quad (1)$$

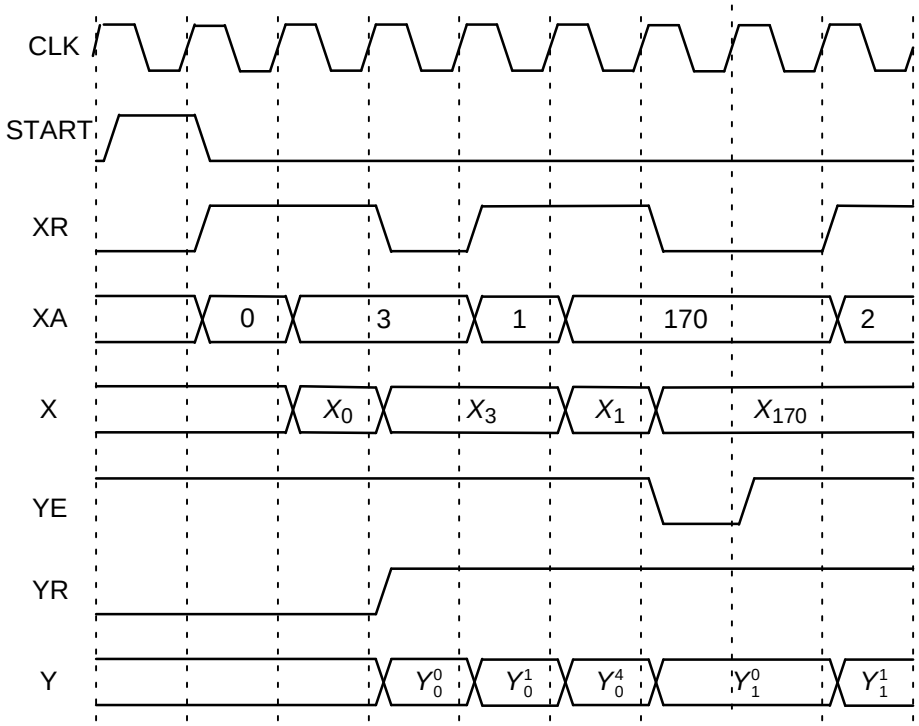

Figure 3: PCE04C Initial Encoder Timing (K = 1784, R = 1/3).

where n is the number of coded bits (2 to 7) and $f_E = 1/T_{cp}$ is the encoder clock speed.

Ordering Information

SW–PCE04C–SOS (SignOnce Site License)
SW–PCE04C–SOP (SignOnce Project License)
SW–PCE04C–VHD (VHDL ASIC License)

All licenses include Xilinx VHDL cores. The SignOnce and ASIC licenses allows unlimited instantiations and free updates for one year.

Note that *Small World Communications* only provides software and does not provide the actual devices themselves. Please contact *Small World Communications* for a quote.

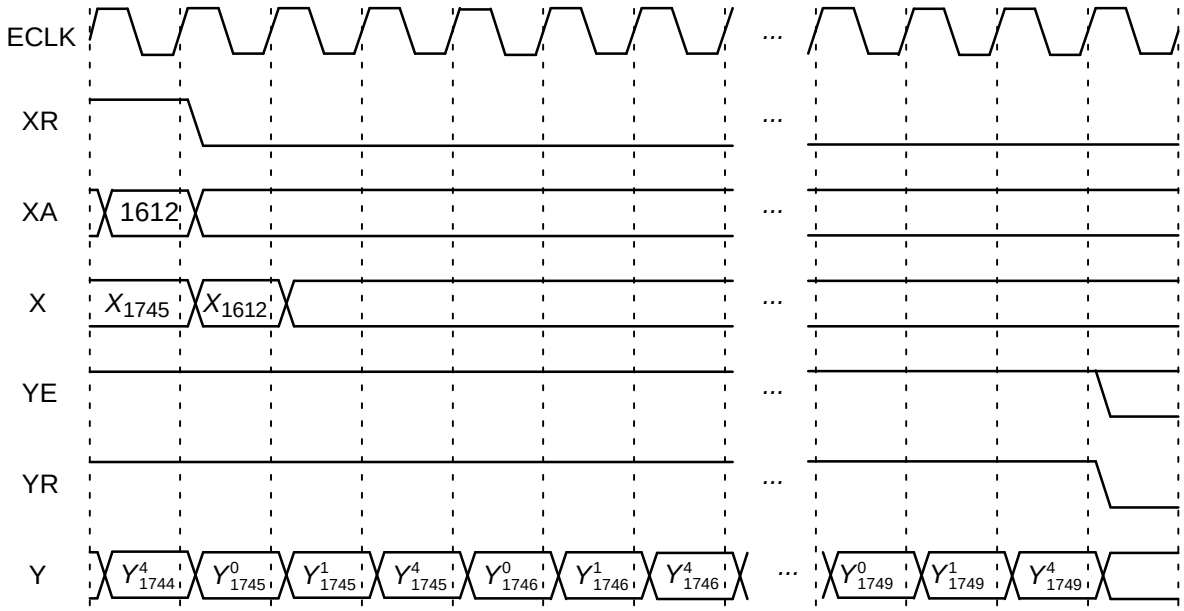

Figure 4: PCE04C Tail Encoder Timing (K = 1784, R = 1/3).

References

[1] Consultive Committee for Space Data Systems, “Recommendation for space data system standards: TM Synchronization and channel coding,” CCSDS 131.0–B–1, Blue Book, Sep. 2003.

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Revision History

- 1.00 25 July 2008. First release
- 1.02 4 Oct. 2010. Deleted Virtex–II performance. Updated Virtex–5 performance. Added Spartan–6 and Virtex–6 performance. Updated Virtex–5 complexity.
- 1.03 7 Dec. 2017. Added Revision History. Deleted Spartan–3, Spartan–6 and Virtex–4 performance. Updated Virtex–5 and Virtex–6 performance. Added Zync–7, Artix–7 and Kintex–7 performance. Deleted Virtex–II and Virtex–5 complexity. Added Kintex–7 complexity. Corrected XA in Figure 3. Corrected (1) and K in Figures 3 and 4.