PCE03V Features

- 8 state 3GPP™ (UMTS and LTE) and 3GPP2 (cdma2000/1xEV–DV Release D and 1xEV–DO Release B) compatible turbo encoder
- Rate 1/2, 1/3, 1/4 or 1/5
- 40 to 5114 (3GPP™ UMTS), 40 to 6144 (3GPP™ LTE) or 17 to 32768 (3GPP2) bit interleaver
- Implement one, two or four different standards from the one core
- Up to 278 MHz internal clock
- Up to 138 Mbit/s encoding speed
- Serial continuous encoded data out
- Available as VHDL core for Xilinx FPGAs under SignOnce IP License. ASIC, Altera, Lattice and Microsemi cores available on request.

Introduction

The PCE03V is an 8 state 3GPP™ (UMTS [1] and LTE [2]) and 3GPP2 (1xEV–DV Release D [3] and 1xEV–DO Release B [4]) compatible turbo encoder. The 3GPP™ and 3GPP2 turbo codes have a number of similarities, but also important differences which affect their implementation. The biggest similarity is that they use the same constituent 8 state systematic recursive convolutional code. The interleavers of 3GPP™ UMTS and 3GPP2 also use a similar row/column architecture, but are quite different in their complexity. 3GPP™ LTE uses a simple quadratic permutation interleaver. The 3GPP™ and 3GPP2 codes also have different tails.

The 3GPP™ UMTS interleaver has either 5, 10 or 20 rows and a number of columns equal to p–1, p or p+1, where p is a prime number from 7 to 257. The 3GPP2 interleaver has 32 rows and 2^n columns, where n ranges from 2 to 10.

For 3GPP™ UMTS, the use of prime numbers and other complexities implies that a number of parameters need to be calculated before the interleaver can be used. When the block length is changed, the interleaver parameters are automatically calculated using an efficient internal circuit. Encoding operations are halted for a short time while the parameters are being calculated. The block length can range from 40 to 5114 bits.

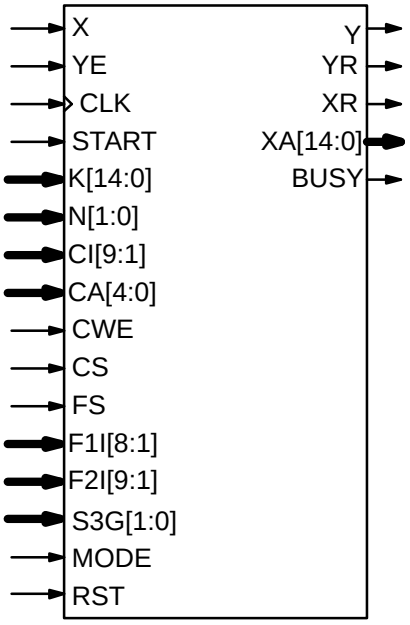

Figure 1: PCE03V schematic symbol.

For 3GPP2, the use of powers of 2 greatly simplifies parameter calculation. The block length can range from 17 to 32768 bits, although the 3GPP2/1xEV–DV standard only uses 23 specific interleavers (186, 378, 402, 570, 762, 786, 1146, 1530, 1554, 2298, 3066, 3090, 4602, 4626, 6138, 6162, 9210, 9234, 12282, 12306, 15378, 18450 and 20730 bits). The forward link for 1xEV–DO uses eight different interleavers (122, 250, 506, 1018, 2042, 3066, 4090, and 5114 bits). The reverse link for 1xEV–DO uses 12 different interleavers (122, 250, 506, 762, 1018, 1530, 2042, 3066, 4090, 6138, 8186, and 12282 bits). For interleaver sizes less than 65, the parameter n is fixed at 2 (4 columns).

For 3GPP™ only a code rate of 1/3 is specified. However, the PCE03V can also optionally encode rate 1/2, 1/4 and 1/5 turbo codes. The encoded data is output in a continuous serial stream, with no pauses in the data for both 3GPP™ and 3GPP2 encoders. For 3GPP2, rate 1/2, 1/3, 1/4 and 1/5 are specified.

For 3GPP™ LTE, there are 188 interleaver sizes ranging from 40 to 6144 bits. Two parameters f_1 and f_2 are used by the interleaver. All interleaver sizes from 40 to 504 bits that are a multiple

of 8, 512 to 1008 bits that are a multiple of 16, 1024 to 2016 bits that are multiple of 32, and 2048 to 6144 bits that are a multiple of 64 are specified.

For 3GPP™, each tail of the two constituent encoders are terminated using all the data and parity bits (for a total of 12 bits for rate 1/3). For rate 1/2 the PCE03V uses the same tail as for rate 1/3. For rate 1/4 and 1/5, a total of 18 tail bits are used.

For 3GPP2, the number of tail bits is equal to 6*n*, for a rate 1/*n* code. For rate 1/2, the tails for 3GPP™ and 3GPP2 are determined in the same way. For rate 1/3 and 1/4 though, data bits are repeated to make up for the additional tail bits in the 3GPP2 standard. For rate 1/5 the data bit is repeated three times for 1xEV–DV and two times for 1xEV–DO. The second parity bit is repeated two times for 1xEV–DO.

Figure 1 shows the schematic symbol for the PCE03V encoder. The VHDL core can be used with Xilinx Integrated Software Environment (ISE) or Vivado software to implement the core in Xilinx FPGA's.

Table 1 shows the performance achieved for various Xilinx parts with $K = 5114$ and 3GPP™ encoding. T_{cp} is the minimum clock period over recommended operating conditions. These performance figures may change due to device utilisation and configuration.

Table 1: Example performance (3GPP™ UMTS)

Part	T_{cp} (ns)	Speed (Mbit/s)			
		1/2	1/3	1/4	1/5
XC5VLX30–1	6.002	83.1	55.4	41.6	33.2
XC5VLX30–2	5.089	98.0	65.4	49.0	39.2
XC5VLX30–3	4.533	110.1	73.4	55.0	44.0
XC6VLX75T–1	4.869	102.5	68.3	51.2	41.0
XC6VLX75T–2	4.230	117.9	78.7	59.0	47.2
XC6VLX75T–3	3.758	132.8	88.5	66.4	53.1
XC7Z010–1	7.270	68.6	45.7	34.3	27.4
XC7Z010–2	5.928	84.1	56.1	42.1	33.7
XC7Z010–3	5.248	95.1	63.4	47.5	38.0
XC7A35T–1	7.109	70.2	46.8	35.1	28.1
XC7A35T–2	5.774	86.4	57.6	43.2	34.6
XC7A35T–3	5.122	97.4	65.0	48.7	39.0
XC7K70T–1	4.826	103.4	68.9	51.7	41.4
XC7K70T–2	3.876	128.7	85.8	64.4	51.5
XC7K70T–3	3.591	138.9	92.7	69.5	55.6

Signal Descriptions

BUSY Initialising Interleaver
CA 3GGP2 row constant address (0 to 31)
CI 3GPP2 row constant (0 to 511)
CS 3GPP2 row constant select
0 = Select internal row constants
1 = Select programmed row constants
CWE 3GPP2 row constant write enable
CLK Encoder Clock
F1I LTE external parameter 1 (0 to 255)
F1I = f_1 div 2.
F2I LTE external parameter 2 (0 to 511)
F2I = f_2 div 2.
FS LTE external parameter select
0 = Select internal parameters
1 = Select external parameters
K Interleaver Length
MODE 0 = small interleaver (K[14:13] = 0)
1 = large interleaver
N Code Rate
2 = rate 1/2
3 = rate 1/3
0 = rate 1/4
1 = rate 1/5
RST Synchronous Reset
S3G 0 = 3GPP™ UMTS
1 = 3GPP™ LTE
2 = 3GPP2/1xEV–DV
3 = 3GPP2/1xEV–DO
START Encoder Start
X Data In
XA Data In Address
XR Data In Ready
Y Data Out
YE Data Out Enable
YR Data Out Ready

Table 2 shows the resources used for Kintex–7. Resources for Virtex–5, Virtex–6 and other 7–Series devices are similar to that for Kintex–7. The complexity does not include the input memory. Only one global clock is used. No other resources are used.

Table 2: Encoder complexity

S3G[1:0]	Mode	6–Input LUTs
GND,GND	3GPP™ UMTS	537
VCC,GND	3GPP2 1xEV–DV	367
PIN,GND	3GPP™ UMTS/ 3GPP2 1xEV–DV	731
GND,VCC	3GPP™ LTE	268

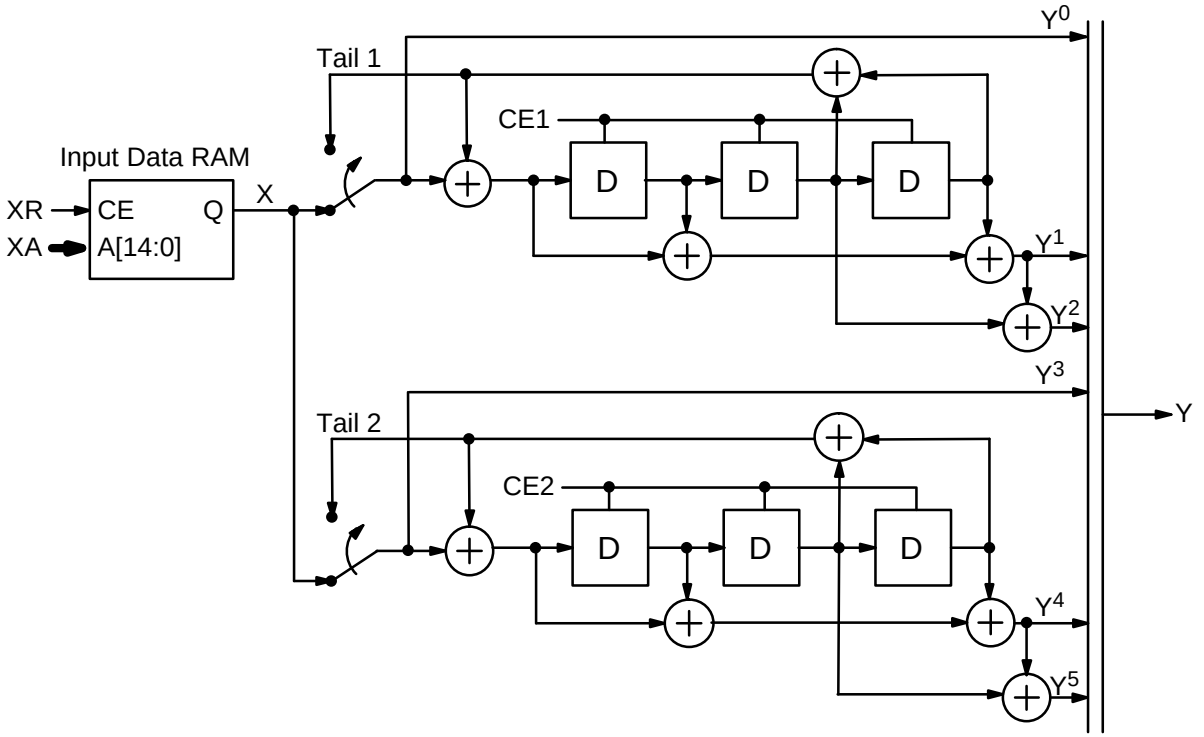

Figure 2: PCE03V eight state turbo encoder.

Table 3 shows how to configure the encoder for the four implementation modes. PIN implies the input is connect to a pin or the output of other logic. MODE should only be connected to VCC or GND, otherwise, excessive implementation complexity and low clock speed will result.

Table 3: Encoder mode

Mode	S3G[1:0]	MODE	K[14:12]	N[1:0]
UMTS	00	0	00,PIN	11
LTE	01	0	00,PIN	11
1xEV–DV	10	1	PIN	PIN
1xEV–DO Forward	11	0	00,PIN	PIN
1xEV–DO Reverse	11	1	0,PIN	PIN
UMTS/ 1xEV–DV	PIN,0	1	PIN	PIN

Encoder

Figure 2 gives a block diagram of the PCE03V 3GPP™/3GPP2 eight state turbo encoder. X is the data input and Y0 to Y5 are the coded outputs. Data is clocked during the low to high transition of CLK. Separate internal clock enables (CE1 and CE2) are used to clock the data into each encoder. Non–interleaved data is clocked into the first encoder and interleaved data is clocked into the second encoder. The twin vertical lines indicate a multiplexer.

The data is input in the sequence X_k $X_{I(k)}$ where X_k is the data at time k from 0 to K–1 and $I(k)$ is the interleaved address. Table 4 shows the output sequence for the various code rates. For rate 1/3 and 1/5, k is incremented by one from 0 to K–1. For rate 1/2 and 1/4, k is incremented by two.

Table 4: Output sequence

Rate	Sequence
1/2	Y^0_k Y^1_k Y^0_{k+1} Y^4_{k+1}
1/3	Y^0_k Y^1_k Y^4_k
1/4	Y^0_k Y^1_k Y^2_k Y^5_k Y^0_{k+1} Y^1_{k+1} Y^4_{k+1} Y^5_{k+1}
1/5	Y^0_k Y^1_k Y^2_k Y^4_k Y^5_k

Note that the output for all rates is output in one continuous stream. The encoder does not pause (unless YE goes low) in outputting the data.

The tail bits are then output. For 3GPP™ and rate 1/2 and 1/3, six bits for the first encoder and six bits for the second encoder. For rate 1/4 and 1/5, nine bits for the first encoder and nine bits for the second encoder. For 3GPP2 and rate 1/n, 3n for the first encoder and 3n for the second encoder are output. Table 5 gives the output sequences for the tails. For example, $(0,1)^3$, $(3,4)^3$ implies the following output sequence: Y^0_K Y^1_K Y^0_{K+1} Y^1_{K+1} Y^0_{K+2} Y^1_{K+2} Y^3_K Y^4_K Y^3_{K+1} Y^4_{K+1} Y^3_{K+2} Y^4_{K+2}. The data is not read while the tails are being generated.

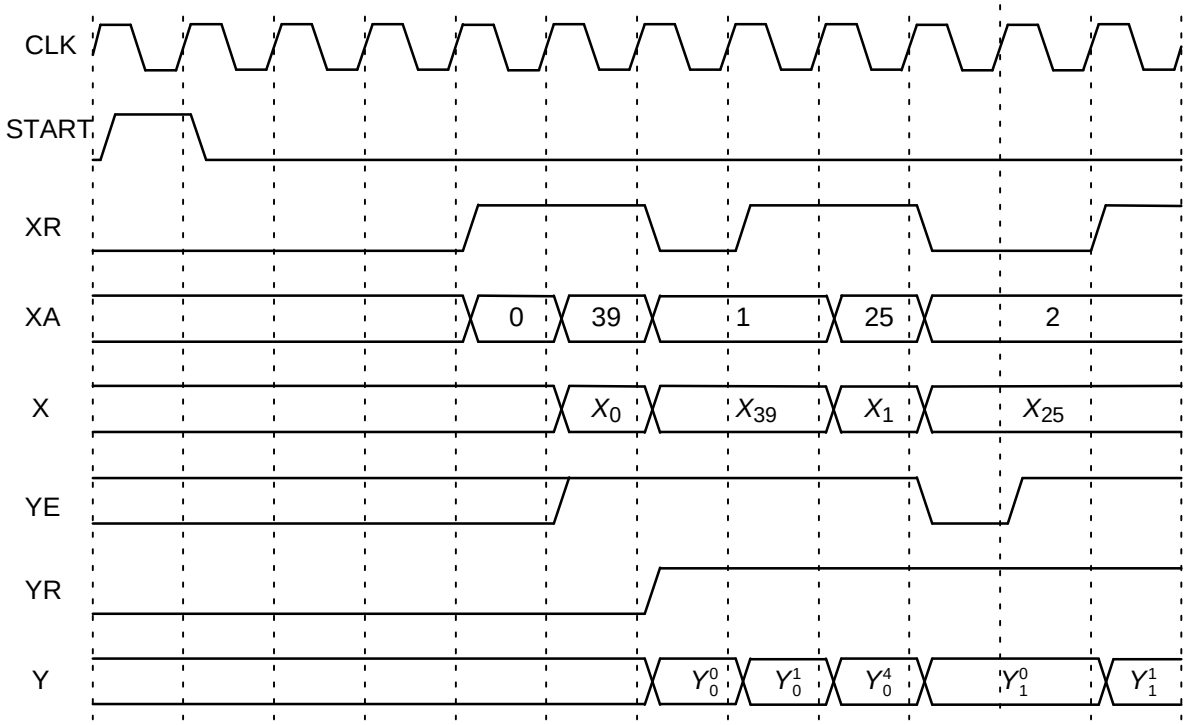

Figure 3: PCE03V Initial Encoder Timing (K = 40, R = 1/3, 3GPP™ UMTS).

Table 5: Tail sequence

Rate	**Sequence (3GPP™)**
1/2,1/3	$(0,1)^3$, $(3,4)^3$
1/4,1/5	$(0,1,2)^3$, $(3,4,5)^3$

Rate	**Sequence (3GPP2)**
1/2	$(0,1)^3$, $(3,4)^3$
1/3	$(0,0,1)^3$, $(3,3,4)^3$
1/4	$(0,0,1,2)^3$, $(3,3,4,5)^3$
1/5	$(0,0,0,1,2)^3$, $(3,3,3,4,5)^3$ 1xEV–DV
1/5	$(0,0,1,2,2)^3$, $(3,3,4,5,5)^3$ 1xEV–DO

Figure 3 shows the initial timing diagram for encoding a block of data of length K = 40 with R=1/3 and S3G = 0 (3GPP™ UMTS). The encoder starts and ends in state 0. When the encoder requires data X to be read from the input RAM, the data ready signal XR goes high and XA[12:0] (XA[14:13] is not used) selects the data bit. After a START signal is initiated XR goes high after three cycles (this occurs for all rates). It is assumed that the data is stored in a synchronous read RAM with XR used to control the enable input of the RAM. An asynchronous read RAM can also be used by registering the RAM output.

If YE is high, the encoded data ready signal YR goes high five clock cycles after a START signal is initiated (this occurs for all rates). YR is high for both the data block and tail. If YE is low the encoder is held during the next low–to–high transition of CLK. The output of XR also goes low when YE goes low so that the data RAM output is held. Figure 4 shows the encoding process for the tail with K = 40. The encoding processing is the same for S3G = 2 or 3 (3GPP2), except that a different interleaver and tail are used.

The nominal input data rate f_e is

$$f_e = \frac{f_E}{n + (6 + t)/K} \tag{1}$$

where n is the number of coded bits (2 to 5), t is the number of tail bits ($6 + 6\lfloor n/2 \rfloor$ for 3GPP™ or $6n$ for 3GPP2), and $f_E = 1/T_{cp}$ is the encoder clock speed.

If K is changed, the interleaver parameters are internally calculated. For S3G = 0 (3GPP™ UMTS), this can take from 35 clock cycles for K = 40 to 1346 clock cycles for K = 5114. For S3G = 2 or 3 (3GPP2), this takes 33 clock cycles for all values of K. For S3G = 1 (3GPP™ LTE), no extra clock cycles are used and encoding can start immediately. Software for generating test vectors provided with the cores also outputs this delay. While the parameters are being calculated the BUSY signal will go high. If START goes high while BUSY is high, the encoder will wait until BUSY goes low, and then start encoding the data.

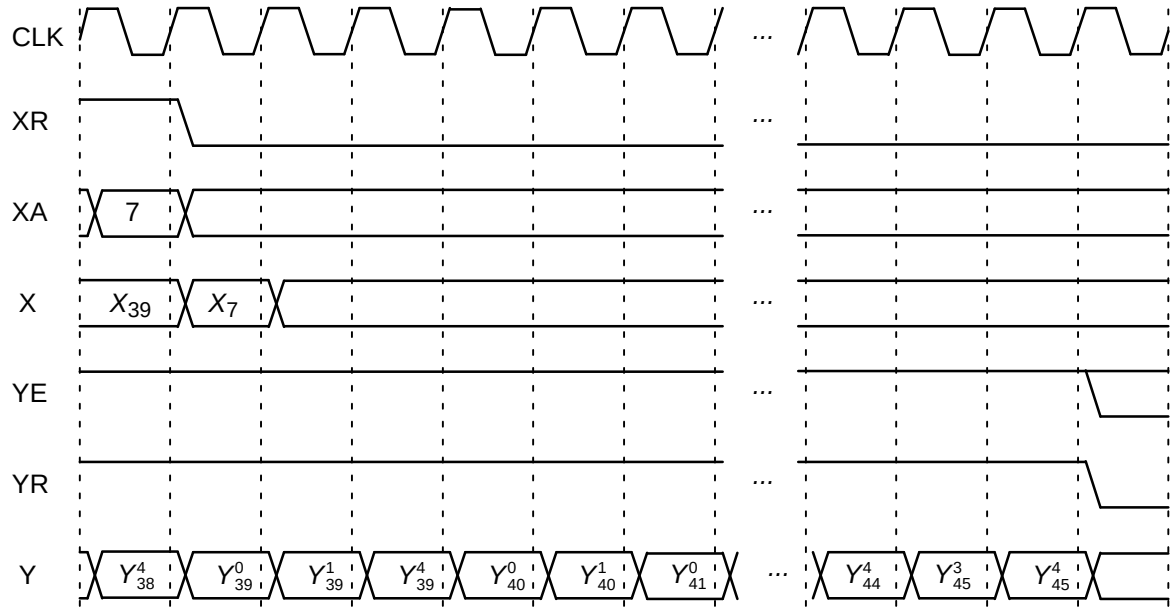

Figure 4: PCE03V Tail Encoder Timing (K = 40, R = 1/3, 3GPP™ UMTS).

3GPP2 Interleaver Programming

The PCE03V turbo encoder allows the option of programming the row constants that are used in the 3GPP2 interleaver. There are 32 constants, all of them being odd in value. Note that if K is the interleaver size, the maximum constant value must be less than 2^n, where $n = \lceil \log_2 K \rceil - 5$.

The maximum value of n is 10, so each constant can be represented by a 10 bit value. However, since all the parameters are odd, this implies the least significant bit (lsb) is always equal to one. Thus, only the nine most significant bits (msb) should be input, with the lsb being ignored. This is why the constant input CI[9:1] does not include the lsb CI0. For example, if the constant is 349, then the lsb should be deleted and $\lfloor 349/2 \rfloor = 174$ be input to CI[9:1].

Figure 5 shows an example of programming the 3GPP2 interleaver parameters. During the low to high transition of CLK, if CWE is high, the value at CI[9:1] is programmed into the internal memory at address location CA[4:0].

Note that K or CS can be changed in any order before, during or after programming the row constants. As long as the correct K and CS are input to the encoder before decoding begins, the encoder will use the selected parameters. If CS is low, the internal 3GPP2 standard parameters are selected. If CS is high, the externally programmed parameters are selected.

3GPP™ LTE Interleaver

There are 188 standard interleaver sizes from 40 to 6144 bits. To select the internal parameters, set FS low and input the data length into K[12:0]. The encoder will automatically select the parameters for that length. Note that the only valid lengths are from 40 to 504 bits that are a multiple of 8, 512 to 1008 bits that are a multiple of 16, 1024 to 2016 bits that are multiple of 32, and 2048 to 6144 bits that are a multiple of 64. Other interleaver lengths will cause incorrect operation.

To input external interleavber parameters, set FS high. Any length from 40 to 6144 bits can be input, provided that K is a multiple of 8. Parameter

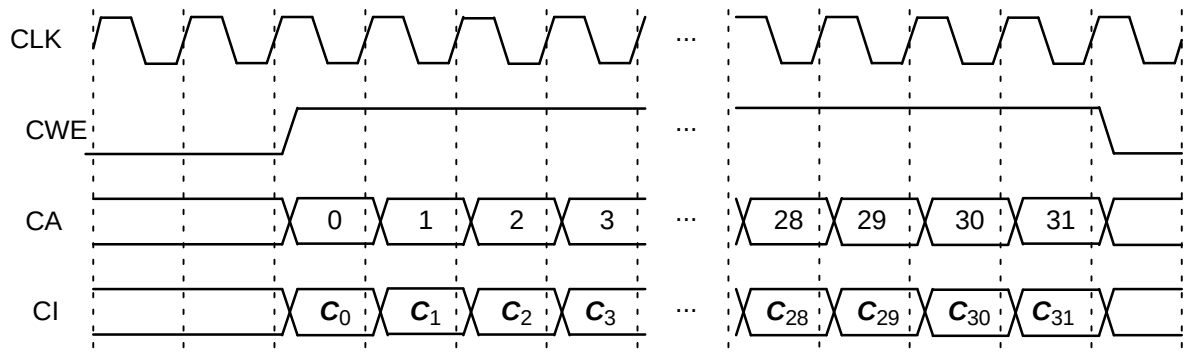

Figure 5: 3GPP2 Parameter Programming.

F1I[8:1] is equal to f_1 divided by two. That is, the least significant bit of f_1 is deleted since it is always equal to one due to f_1 being odd. Similarly, parameter F2I[9:1] is equal to f_2 divided by two since f_2 is always even. For correct operation, $f_1 < 512$, $f_2 < 1024$, and $f_1+f_2 < 1024$.

Ordering Information

SW–PCE03V–SOS (SignOnce Site License)
SW–PCE03V–SOP (SignOnce Project License)
SW–PCE03V–VHD (VHDL ASIC License)

All licenses include Xilinx VHDL cores. The SignOnce and ASIC licenses allows unlimited instantiations and free updates for one year.

Note that *Small World Communications* only provides software and does not provide the actual devices themselves. Please contact *Small World Communications* for a quote.

References

[1] Third Generation Partnership Project (3GPP), "Universal mobile telecommunications system (UMTS); Multiplexing and channel coding (FDD)," 3GPP TS 25.212 version 5.2.0 Release 5, Sep. 2002.

[2] Third Generation Partnership Project (3GPP), "Evolved universal terrestrial radio access (E–UTRA); Multiplexing and channel coding," 3GPP TS 36.212 V8.1.0 Release 8, Nov. 2007.

[3] Third Generation Partnership Project 2 (3GPP2), "Physical layer standard for cdma2000 spread spectrum systems, Release D," 3GPP2 C.S0002–D Version 1.0, Feb. 2004.

[4] Third Generation Partnership Project 2 (3GPP2), "cdma2000 high rate packet data air interface specification, Release B," 3GPP2 C.S0024–B Version 2.0, Mar. 2007.

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Version History

- 0.0 24 October 2000. Preliminary product specification for rate 1/3 UMTS encoder.
- 0.2 25 November 2000. Deleted YA[13:0] output. Changed CLK to ECLK. Changed WE from active low to rising edge. Added encoding speed. Added Encoder, Bit and MCS Files, Configuration, Pinouts, Packages, Ordering Information, References and Switching Characteristics sections. Added encoder and timing diagrams.
- 0.4 10 August 2001. Added INIT and RST input pins and BUSY output pin. Changed MA[1:0] to MA[5:0]. Changed Interleaver Parameter section to Interleaver Programming section. Added Appendix section. s(0) to s(p–2) now internally calculated using external nu.
- 0.5 20 September 2002. Deleted parameter programming inputs. All UMTS interleaver parameters now internally calculated. Added N[1:0] input. Deleted Interleaver Programming, Bit and MCS Files, Configuration, Pinouts, Packages, Appendix and Switching Characteristics sections. Added rate 1/2, 1/4 and 1/5 encoding options.

- 1.0 8 November 2002. First official release. Added S3G and MODE inputs. Changed K[12:0] and XA[12:0] to K[14:0] and XA[14:0]. Added 3GPP2 1xEV–DV optional encoding. Added Virtex–II speed and complexity.
- 1.1 13 January 2003. Minor updates.
- 1.21 15 February 2005. Updated speed and complexity. Added Spartan–3 speed.
- 1.22 26 May 2005. Added Virtex–II Pro and Virtex–4 speed. Updated Virtex–II and Spartan–3 speed. Updated UMTS Virtex–II family complexity.
- 1.3 16 May 2006. Changed S3G to S3G[1:0]. Added 3GPP2 1xEV–DO optional encoding. Updated Virtex–II family complexity. Updated complexity.
- 1.31 4 April 2007. Minor updates.
- 1.40 11 July 2008. Added CI[9:1], CA[4:0], CWE, CS, FS, F1I[8:1] and F2I[9:1] inputs. Added 3GPP™ LTE optional encoding and 3GPP2 optional parameter programming. Deleted Virtex–E and Virtex–II speed. Deleted Virtex family complexity. Added Virtex–5 speed and complexity. Updated Virtex–II family complexity.
- 1.43 26 November 2010. Deleted Virtex–II speed. Updated Spartan–3, Virtex–4 and Virtex–5 speed. Added Spartan–6 and Virtex–6 speed. Updated Virtex–4 and Virtex–5 complexity. Deleted BlockRAM for UMTS.
- 1.44 10 March 2017. Changed ECLK to CLK. Changed 3GPP2 internal parameter calculation time from 32 to 33 clock cycles. Deleted Spartan–3, Spartan–6 and Virtex–4 speed. Updated Virtex–5 and Virtex–6 speed. Added Artix–7, Kintex–7 and Zync–7 speed. Deleted Virtex–4 complexity and university license option. Added Version History section.
- 1.45 16 March 2017. Updated performance and complexity.
- 1.46 11 July 2017. Updated performance and complexity.