



### PCE03D Features

- 8 state DVB-RCS and IEEE 802.16 WiMAX compatible
- Rate 1/3, 2/5, 1/2, 2/3, 3/4, 4/5, 5/6, 6/7, 7/8 with reverse output option
- Automatic puncturing
- 48 to 2048 or 5120 bit data length
- Up to 270 Mbit/s encoding speed
- 2-bit or 6-bit parallel encoded data out
- DVB-RCS or IEEE 802.16 WiMAX implementation options with optional interleaver parameters
- Available as EDIF core and VHDL simulation core for Xilinx FPGAs under SignOnce IP License. Actel, Altera and Lattice FPGA cores available on request.
- Available as VHDL core for ASICs

### Introduction

The PCE03D is an 8 state DVB-RCS [1] and IEEE 802.16 WiMAX [2] compatible turbo encoder. Encoded data is output 2-bits or 6-bits in parallel for increased speed. Optional external interleaver parameters can be used. The turbo code uses an eight state rate 2/4 systematic recursive convolutional tail-biting constituent code. Since a tail-biting code is used, there are no tail bits, increasing the bandwidth efficiency of the code. For DVB-RCS, block sizes from 96 to 1728 are used. For IEEE 802.16 WiMAX, block sizes range from 48 to 4800 bits.

The interleavers for the standards are similar, using linear congruential equations that depend on four parameters, P0I to P3I.

With IEEE 802.16 WiMAX, there are two different interleavers, depending on the system used; WirelessMAN-OFDM and WirelessMAN-OFDMA.

Figure 1 shows the schematic symbol for the PCE03D encoder. The EDIF core can be used with Xilinx Integrated Software Environment (ISE) software to implement the core in Xilinx FPGA's. The VHDL core can be used in ASIC designs.

Table 1 shows the resources used for various Virtex-4 and Virtex-5 devices. Resources for Virtex-II and Spartan-3 devices are similar to that for Virtex-4. Resources for Virtex-6, Spartan-6 and

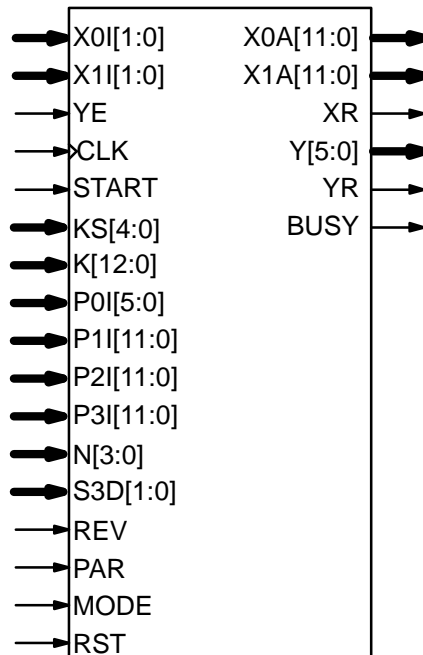


Figure 1: PCE03D schematic symbol.

7-Series devices are similar to that for Virtex-5. The MODE input can be used to select various encoder implementations. The input/output memory is not included. Only one global clock is used. No other resources are used.

Table 1: Resources used.

Configuration	Virtex-4 LUTs	Virtex-5 LUTs
DVB-RCS	469	340
WiMAX	424	324

Table 2 shows the performance achieved with 6-bit or 2-bit forward output, rate 1/2 and  $K = 4800$  and 2-bit reverse output, rate 1/3 and  $K = 1728$  for various Xilinx parts.  $T_{cp}$  is the minimum clock period over recommended operating conditions. These performance figures may change due to device utilisation and configuration.

Only one global clock is used. No other resources are used except for the external input memory.

### Signal Descriptions

- BUSY Encoder busy
- CLK Clock

**Table 2: Example performance**

Part	T <sub>cp</sub> (ns)	Speed <sup>1</sup> (Mbit/s)	Speed <sup>2</sup> (Mbit/s)
XC6SLX4-2	8.309	120.3	60.1
XC6SLX4-3	7.093	140.9	70.4
XC4VFX12-10	8.457	118.1	59.0
XC4VFX12-11	7.207	138.6	69.3
XC4VFX12-12	6.403	156.0	78.0
XC5VLX30-1	6.273	159.3	79.6
XC5VLX30-2	5.386	185.6	92.8
XC5VLX30-3	4.807	207.9	103.9
XC6VLX75T-1	4.676	213.7	106.8
XC6VLX75T-2	4.146	241.0	120.5
XC6VLX75T-3	3.692	270.7	135.3
XC7A100T-1	6.614	151.0	75.5
XC7A100T-2	5.403	184.9	92.4
XC7A100T-3	4.813	207.6	103.7
XC7K30T-1	4.987	200.4	100.2
XC7K30T-2	4.277	233.7	116.8
XC7K30T-3	3.684	271.3	135.6

<sup>1</sup> Rate = 1/2, K = 4800, 6-bit or 2-bit forward

<sup>2</sup> Rate = 1/3, K = 1728, 2-bit reverse

**K** Data Length (Minimum = 48. Maximum = 2048 with MODE = 0 and 5120 with MODE = 1)

**KS** Data Length Select

0 = select K, P0I-P3I

S3D = 0 (DVB-RCS)

1 = length 96 (12 bytes)

2 = length 128 (16 bytes)

3 = length 424 (53 bytes)

4 = length 440 (55 bytes)

5 = length 456 (57 bytes)

6 = length 848 (106 bytes)

7 = length 864 (108 bytes)

8 = length 880 (110 bytes)

9 = length 1696 (212 bytes)

10 = length 1712 (214 bytes)

11 = length 1728 (216 bytes)

12 = length 1504 (188 bytes)

S3D = 3 (WirelessMAN-OFDMA)

1 = length 48 (6 bytes)

2 = length 96 (12 bytes)

3 = length 144 (18 bytes)

4 = length 192 (24 bytes)

5 = length 240 (30 bytes)

6 = length 288 (36 bytes)

7 = length 384 (48 bytes)

8 = length 432 (54 bytes)

9 = length 480 (60 bytes)

10 = length 72 (9 bytes)

11 = length 216 (27 bytes)

12 = length 360 (45 bytes)

13 = length 960 (120 bytes)

14 = length 1920 (240 bytes)

15 = length 2880 (360 bytes)

16 = length 3840 (480 bytes)

17 = length 4800 (600 bytes)

**MODE** Mode select

0 = 1K Interleaver (DVB-RCS)

1 = 2.5K Interleaver (WiMAX)

**N** Code Rate

0 = rate 1/2

1 = rate 2/3

2 = rate 3/4

3 = rate 4/5

4 = rate 5/6

5 = rate 6/7

6 = rate 7/8

8 = rate 1/3

9 = rate 2/5

**PAR** Parallel Encoded Data Select

0 = 2-bit

1 = 6-bit

**REV** Reverse data output

0 = Input data output first

1 = Input data output last

**RST** Synchronous Reset

**S3D** Code Select

0 = DVB-RCS

2 = IEEE 802.16 WirelessMAN-OFDM

3 = IEEE 802.16 WirelessMAN-OFDMA

**START** Encoder Start

**X0I** Non-interleaved Data In

**X1I** Interleaved Data In

**X0A** Non-interleaved Data In Address

**X1A** Interleaved Data In Address

**XR** Data In Ready

**Y** Encoded Data Out (data and parity)

**YE** Encoded Data Out Enable

**YR** Data Out Ready

Note that MODE is a "soft" input and should not be connected to input pins or logic. This input is designed to minimise decoder complexity for the configuration selected.

## Encoder

Figure 2 gives a block diagram of the PCE03D DVB-RCS eight state turbo encoder. X0I[1:0] and X1I[1:0] are the data and interleaved data input, respectively and Y[1:0] (PAR = 0) or Y[5:0] (PAR = 1) are the coded outputs. Data is clocked during the low to high transition of CLK. In the first K/2

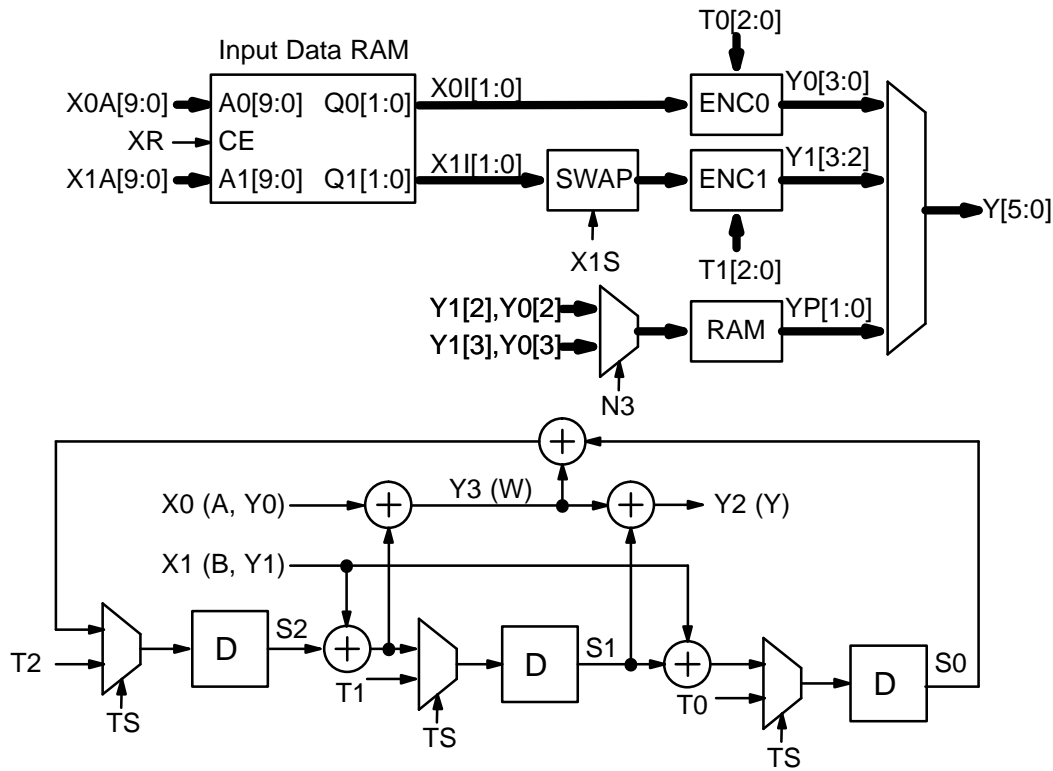


Figure 2: PCE03D DVB-RCS/WiMAX eight state turbo encoder.

clock cycles, data is input to the encoders starting from state 0. The final state of this sequence along with the value of  $K/2 \bmod 7$ , determines the tail-biting state  $T[2:0]$  which is selected by TS. Note that if  $K/2$  is divisible by 7 ( $K/2 \bmod 7 = 0$ ) then tail-biting is not possible for all input sequences. In the following  $K/2$  to  $3K/2$  clock cycles, encoded data is produced. For punctured codes, parity data is stored in the RAM so that it can then be sequentially read out.

Let  $\mathbf{X}_k = \{X_k^0, X_k^1\} = \{Y_{0,k}^0, Y_{0,k}^1\} = \{A_k, B_k\}$  be the input data to  $X0I[1:0]$  at time  $k$ , from 0 to  $K-1$ . The input data to  $X1I[1:0]$  is  $\mathbf{X}_{l(k)} = \{X_{l(k)}^0, X_{l(k)}^1\} = \{Y_{1,k}^0, Y_{1,k}^1\} = \{A_{l(k)}, B_{l(k)}\}$  where  $l(k)$  is the interleaved address,  $l(k) = (k+h) \bmod 2$ ,  $h = 1$  for DVB-RCS and WirelessMAN-OFDMA and  $h = 0$  for WirelessMAN-OFDM. The term  $Y_{j,k}^i$  refers to the coded output at time  $k$ ,  $i$  is the index of the coded bit ( $0 \leq i \leq 3$ ) and  $j$  indicates whether the coded sequence corresponds to an interleaved input of  $\mathbf{X}_k$ , i.e., if  $j = 0$  the input data is  $\mathbf{X}_k$  and if  $j = 1$  the input data is  $\mathbf{X}_{l(k)}$ . The terms  $\{A_k, B_k\}$  corresponds to the notation used in the standard.

Let  $\mathbf{Y}_k^2 = \{Y_{0,k}^2, Y_{1,k}^2\} = \{Y_{1,k}, Y_{2,k}\}$  and  $\mathbf{Y}_k^3 = \{Y_{0,k}^3, Y_{1,k}^3\} = \{W_{1,k}, W_{2,k}\}$  be the first and second coded parity bits, respectively, each corresponding to non-interleaved and interleaved input data.

The terms  $\{Y_{1,k}, Y_{2,k}\}$  and  $\{W_{1,k}, W_{2,k}\}$  corresponds to the notation used in the standard.

Table 3 shows the 2-bit output (PAR = 0) delay and output sequence depending on the code rate and whether the reverse output mode is selected. The additional three clock cycles are due to the START input and then a two clock cycle pipeline delay. For 6-bit output (PAR = 1) the delay is  $K/2+3$  and the encoding time is  $K+3$ .

Table 3: Output Sequence for 2-bit Output

REV	Rates	Delay	Sequence	Time (T)
0	1/2	3	$\mathbf{X Y}^2$	$K+3$
0	2/3-7/8	$K/2+3$	$\mathbf{0 X Y}^2$	$K+L_2+3$
0	1/3	3	$\mathbf{X Y}^2 \mathbf{Y}^3$	$1.5K+3$
0	2/5	$K/2+3$	$\mathbf{0 X Y}^2 \mathbf{Y}^3$	$1.5K+L_3+3$
1	1/2	$K/2+3$	$\mathbf{0 Y}^2 \mathbf{X}$	$1.5K+3$
1	2/3-7/8	$K+3$	$\mathbf{0 0 Y}^2 \mathbf{X}$	$1.5K+L_2+3$
1	1/3-2/5	$K/2+3$	$\mathbf{0 Y}^2 \mathbf{Y}^3 \mathbf{X}$	$1.5K+L_3+3$

The terms  $\mathbf{X} = \{X_0, \dots, X_{K/2-1}\}$ ,  $\mathbf{Y}^2 = \{Y_{p_2,k}^2, 0 \leq k \leq L_2-1\}$ ,  $\mathbf{Y}^3 = \{Y_{p_3,k}^3, 0 \leq k \leq L_3-1\}$  and  $\mathbf{0} = \{0,0, 0 \leq k \leq K/2-1\}$  are used to describe the coded sequence outputs where  $p_2$  and  $p_3$  correspond to the puncturing period for each parity bit and  $L_i = \lceil K/(2p_i) \rceil$ ,  $2 \leq i \leq 3$  correspond to the lengths of the punctured sequences. Let the nomi-

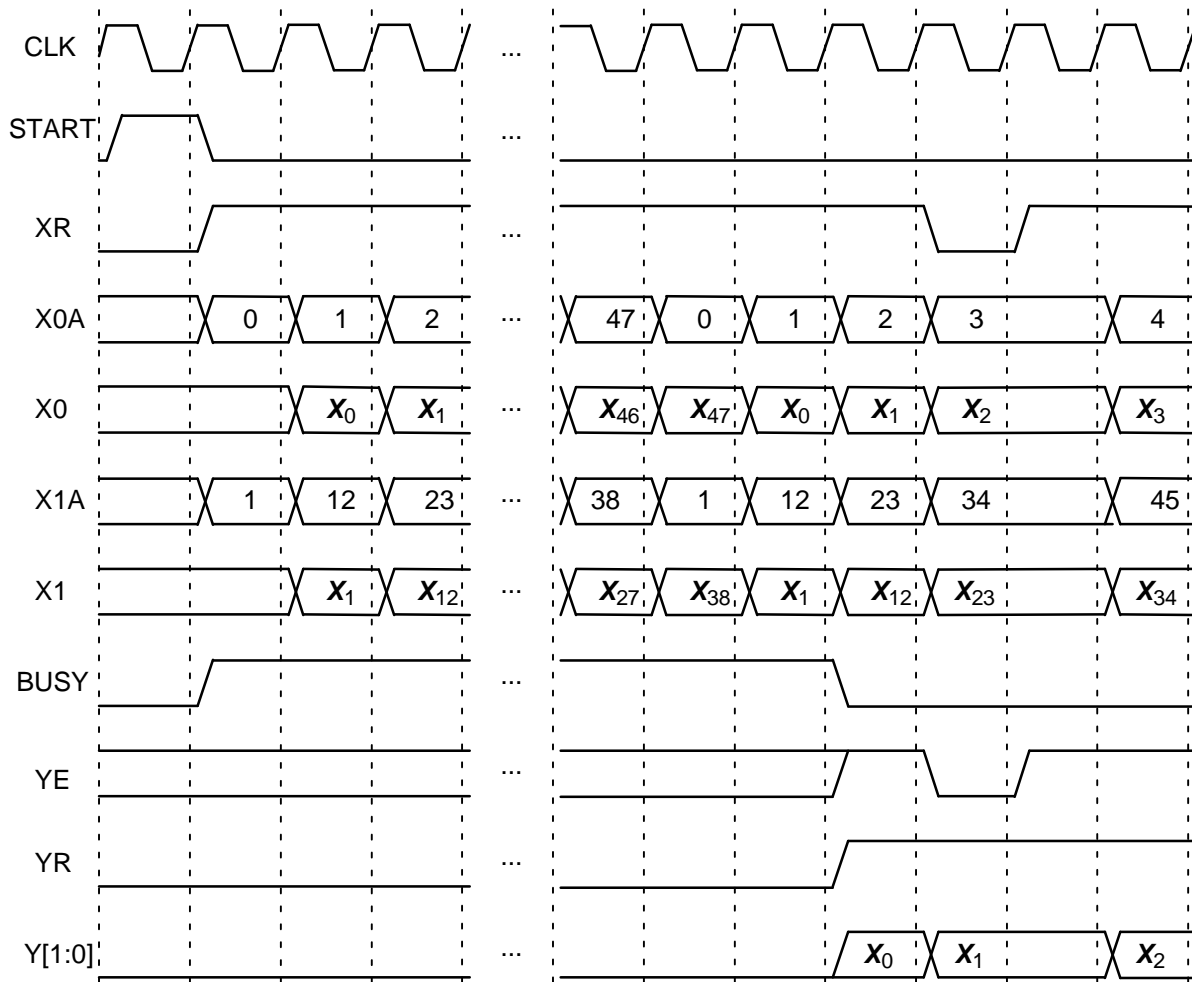


Figure 3: PCE03D Initial Encoder Timing ( $K = 96$ ,  $R = 2/3$ , 2-bit forward DVB-RCS).

nal code rate be  $p/n$ . Then for rates  $1/2$  to  $7/8$  we have  $p_2 = p$  ( $Y^3$  is not output so  $p_3$  is not defined). For rates  $1/3$  and  $2/5$  we have  $p_2 = 1$  and  $p_3 = p$ .

Table 4 shows the relationship between the input and output bits and the notation used for  $PAR = 1$ . Note that no puncturing is performed with  $PAR = 1$ , i.e., the inputs  $N[3:0]$  are ignored.

Note that the output is in one continuous stream. The encoder does not pause (unless  $YE$  goes low) in outputting the data.

Figure 3 shows the initial timing diagram for encoding a block of data of length  $K = 96$ . When the encoder requires data  $X0I[1:0]$  and  $X1I[1:0]$  to be read from the input RAM, the data ready signal  $XR$  goes high and  $X0A[11:0]$  and  $X1A[11:0]$  selects the non-interleaved and interleaved data bits. After a  $START$  signal is initiated  $XR$  goes high. It is assumed that the data is stored in a synchronous read dual port RAM (or two single port RAMs) with  $XR$  used to control the enable input of the RAM. An asynchronous read RAM can also be used by registering the RAM output.

Table 4: Input/Output Notation for  $PAR = 1$

PCE03D	Standard	Uniform
X0I[0]	$A_k$	$X_k^0$
X0I[1]	$B_k$	$X_k^1$
X1I[0]	$A_{l(k)}$	$X_{l(k)}^0$
X1I[1]	$B_{l(k)}$	$X_{l(k)}^1$
Y[0]	$A_k$	$X_k^0$
Y[1]	$B_k$	$X_k^1$
Y[2]	$Y_{1,k}$	$Y_{0,k}^2$
Y[3]	$Y_{2,k}$	$Y_{1,k}^2$
Y[2]	$W_{1,k}$	$Y_{0,k}^3$
Y[3]	$W_{2,k}$	$Y_{1,k}^3$

The encoded data ready signal  $YR$  goes high  $2$ ,  $K/2+2$  or  $K+2$  clock cycles after a  $START$  signal is initiated, during which time  $BUSY$  is high. If  $YE$  is low and  $YR$  is high the encoder is held during the next low-to-high transition of  $CLK$ . The output of  $XR$  also goes low when  $YE$  goes low so that the

data RAM output is held. When encoding is completed YR goes low.

The nominal input data rate  $f_e$  is

$$f_e = \frac{f_E K}{T} \quad (1)$$

where  $f_E = 1/T_{CP}$  is the encoder clock speed and  $T$  is the decoding time as given in Table 3 for PAR = 0. For PAR = 1 we have  $T = K+3$ .

### Interleaver parameters

The interleaving equations are of the form  $i = (P_0 j + 1 + Q(j \bmod 4)) \bmod K/2$  where  $j$  varies from 0 to  $K/2-1$ . The input bits  $X1[1:0]$  are reversed in order when  $j \bmod 2 = 0$  for all schemes. Table 5 gives the formulas for  $Q(j)$  for the four interleaver types.

**Table 5: Interleaver Parameters**

$j$	$Q(j)$		
	DVB-RCS	Wire less MAN-OFDM	Wire less MAN-OFDMA
0	0	0	0
1	$K/4+P_1$	0	$K/4+P_1$
2	$P_2$	$K/8$	$P_2$
3	$K/4+P_3$	$K/4+P_1$	$K/4+P_3$

For DVB-RCS and WirelessMAN-OFDMA, the same interleaver is used, although the parameters  $P_0$  to  $P_3$  used for each scheme are different. Also, WirelessMAN-OFDMA has a longer maximum data length (4800 bits), compared to 1728 bits for DVB-RCS.

The parameters  $P_0$  to  $P_3$  depend on the block length  $K$  and which of the four schemes are used. These values are given in the two standards.  $P_0$  is a prime number while  $P_1$  to  $P_3$  are even numbers.

When  $KS[4:0] = 0$ , the data length  $K$  is input to  $K[12:0]$  and the interleaver parameters  $P_0$  to  $P_3$  are input to  $P0I[5:0]$ , and  $P1I[11:0]$  to  $P3I[11:0]$ , respectively.

When  $KS[4:0] > 0$ , the internal data length selected by  $KS$  is used. Also, the internal interleaver parameters  $P_0$  to  $P_3$  for the data length and standard (either DVB-RCS or WirelessMAN-OFDMA) are used. The inputs  $K[12:0]$ ,  $P0I[5:0]$ , and  $P1I[11:0]$  to  $P3I[11:0]$  are ignored.

For WirelessMAN-OFDM,  $P_1 = 3K/8$ , thus  $(K/4+P_1) \bmod K/2 = K/8$ . There are only two parameters  $K$  and  $P_0$ , which are input to  $K[12:0]$  and  $P0I[11:0]$ . The parameter inputs  $P1I[5:0]$  to  $P3I[5:0]$  are ignored. Note that if  $S3D = 2$ , the

value of  $KS$  is also ignored. That is,  $K$  and  $P0I$  have to be externally input.

For WirelessMAN-OFDM,  $K$  depends on the number of subchannels and modulation used (QPSK, 16QAM, or 64QAM). The parameter  $P_0$  depends on the modulation and the code rate (1/2, 2/3, or 3/4) used.

### Ordering Information

SW-PCE03D-SOS (SignOnce Site License)  
 SW-PCE03D-SOP (SignOnce Project License)  
 SW-PCE03D-VHD (VHDL ASIC License)

All licenses include EDIF and VHDL cores. The VHDL cores can only be used for simulation in the SignOnce and University licenses. The SignOnce and ASIC licenses allows unlimited instantiations.

Note that *Small World Communications* only provides software and does not provide the actual devices themselves. Please contact *Small World Communications* for a quote.

### References

- [1] ETSI, "Digital video broadcasting (DVB); Interaction channel for satellite distribution systems," EN 301 790 V1.5.1, May 2009.
- [2] IEEE, "Standard for air interface for broadband wireless access systems," IEEE Std 802.16-2012, 17 Aug. 2012.

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## Version History

- 1.00 31 October 2011. First release.
- 1.01 9 November 2011. Added 6–bit parallel encoded data output option. Reduced delay for PAR=0, REV=0 and rate 1/2 and 1/3. Increased encoder speed. Added Spartan–6, Virtex–6 and Kintex–7 example performance.
- 1.02 8 February 2013. Added REV in Signal Descriptions.
- 1.03 4 June 2015. Corrected WirelessMAN–OFDM interleaver. Added Virtex–4 and Artix–7 performance. Added Table 1 complexity.