MAP03T Features

- 8 state soft–in–soft–out (SISO) maximum a posteriori (MAP) triple interleaved error control decoder and systematic recursive convolutional encoder
- Up to 120 Mbit/s decoding speed
- Rate 1/2, 1/3, or 1/4 with optional punctured inputs
- 6–bit received data, 8–bit soft–in and soft–out data for information and parity bits for all rates
- 8–bit branch metric inputs for rate 1/2
- Optional code polynomials
- Optional block decoding with or without tail
- Optional max–log–MAP or log–MAP algorithm with 9 or 17 programmable SNR's
- Continuous sliding block algorithm with sliding block lengths of 32 or 64
- Low decoding delay (398 or 782 CLK cycles)
- No external RAM required
- Asynchronous logic free design
- Low power mode and synchronous reset
- Ideal for iterative decoding of 3GPP^{TM} turbo codes
- Available as EDIF/VHDL cores or BIT/MCS files for download into Xilinx Virtex, Virtex–E, Virtex–II, Spartan–II, and Spartan–IIE FPGA's. Support for ASIC cores is also available.

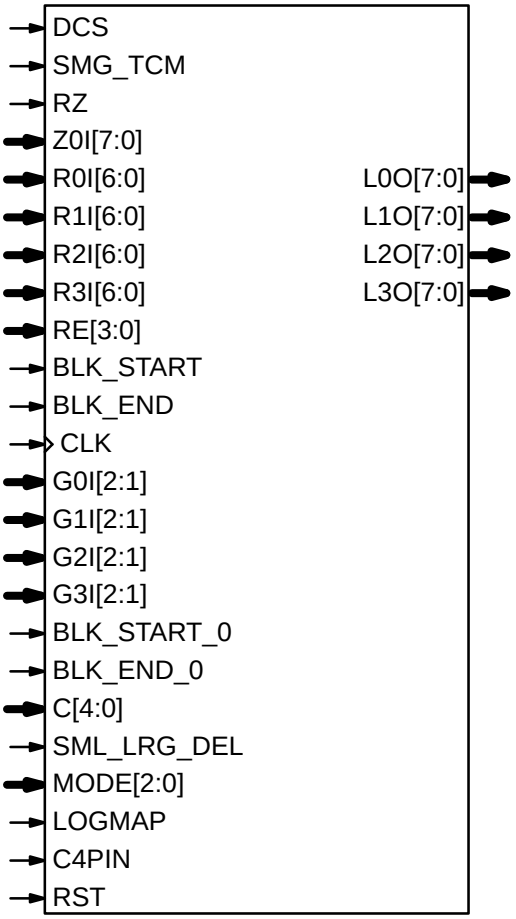

Figure 1: MAP03T schematic symbol.

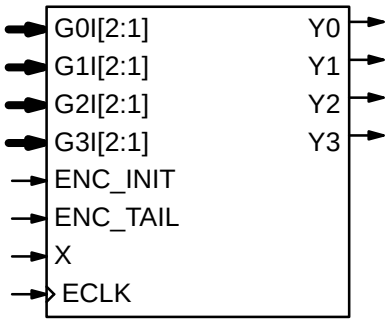

Figure 2: ENC03T schematic symbol.

Introduction

The MAP03T is an 8 state very high speed maximum a posteriori (MAP) soft–in–soft–out (SISO) triple interleaved error control decoder with log–likelihood–ratio outputs for both the data and parity bits. A MAP decoder finds the most likely information bit to have been transmitted given a received noisy or distorted sequence, thus minimising the bit error rate (BER). This is unlike a Viterbi decoder which finds the most likely coded sequence. At low BERs, the MAP and Viterbi algorithms provide almost identical performance. However, at high BERs such as that experienced in iterative "turbo" decoders, MAP decoders can perform approximately 1 dB better than soft–output Viterbi decoder algorithms. A MAP decoder also inherently provides a soft output.

To achieve maximum decoding speed, the MAP03T uses three stages of internal pipelining. This results in a single MAP decoder that is equivalent to three MAP decoders operating in parallel in a triple interleaved structure.

Figures 1 and 2 show the schematic symbols for the MAP03T decoder and ENC03T encoder, respectively. These are the symbols that are used

to compile various BIT files for download into Xilinx FPGA's. These symbols, along with EDIF cores for the ENC03T are freely available for Foundation schematics from [1]. Table 1 shows the various Xilinx parts currently supported. Support for other Xilinx Virtex parts are available on request. Consult the Xilinx data book for a list of devices, speeds, and packages currently available.

Table 1: Xilinx parts currently supported*.

Part No.	Speed (Mbit/s)/Speed Grade		
XCV200E	69.5/–6	77.8/–7	100.1/–8
XC2V500	95.8/–4	110.1/–5	121.2/–6

*Mode 1H, C4PIN low, LOGMAP high

Signal Descriptions (MAP03T)

BLK_END	Block End Signal
BLK_END_0	Block Ends in State 0
BLK_START	Block Start Signal
BLK_START_0	Block Starts in State 0
CLK	System Clock
C4PIN	Maximum C of 9 or 17 (soft)
C[5:0]	MAP decoder constant
DCS	Decoder Chip Select
G0I[2:1]	Code Polynomial for Y0
G1I[2:1]	Code Polynomial for Y1
G2I[2:1]	Code Polynomial for Y2
G3I[2:1]	Code Polynomial for Y3
L0O[7:0]	Log Likelihood Ratio for R0I
L1O[7:0]	Log Likelihood Ratio for R1I
L2O[7:0]	Log Likelihood Ratio for R2I
L3O[7:0]	Log Likelihood Ratio for R3I
LOGMAP	Sub–MAP or Log–MAP (soft)
MODE[2:0]	Decoder Mode
R0I[6:0]	Received Data for Y0
R1I[6:0]	Received Data for Y1
R2I[6:0]	Received Data for Y2
R3I[6:0]	Received Data for Y3
RE[3:0]	Receive Data Enable
RST	Synchronous Reset
RZ	Receive or A Priori Data
SMG_TCM	Signed Magnitude or Two's Complement Data
SML_LRG_DEL	Small or Large Delay
Z0I[7:0]	A Priori Information for Y0

Signal Descriptions (ENC03T)

ECLK	Encoder Clock
ENC_INIT	Block Start Signal
ENC_TAIL	Tail Output Signal
G0I[2:1]	Code Polynomial for Y0
G1I[2:1]	Code Polynomial for Y1
G2I[2:1]	Code Polynomial for Y2
G3I[2:1]	Code Polynomial for Y3
X	Data Input
Y0	Data/Tail Output
Y1	Parity for G1I
Y2	Parity for G2I
Y3	Parity for G3I

Encoder

Figure 3 gives a block diagram of the triple interleaved 8 state systematic recursive encoder available in the ENC03T. The input and output D FF's are not shown. X is the data input and Y0 to Y3 are the coded outputs. GiIj = $g_i^j \in \{0,1\}$, $0 \le i \le 2$, $1 \le j \le 2$, correspond to the code polynomial coefficients which are also used by the decoder. Data is clocked during the low to high transition of ECLK. Note that due to three stages of internal pipelining in the MAP decoder, each delay element (D^3) is equivalent to a length three shift register.

The encoder polynomials are defined as

$$g_i(D) = 1 + g_i^1 D + g_i^2 D^2 + D^3. \quad (1)$$

where D is the delay operator and + indicates modulo–2 (exclusive OR) addition. It is usual practice to express the coefficients in octal notation, e.g., $g_0 = 13_8 = 1011_2 \equiv g_0(D) = 1 + D^2 + D^3$. This corresponds to G0I[2:1] = 10_2.

Figure 4 shows the timing diagram for encoding a block of data of length N, including 9 tail bits (the subscripts indicate the time index). The encoder starts and ends in state 0. The ENC_INIT signal is used to indicate the start of the block and initialises the encoder state to 0 when high and during a low to high transition of ECLK. The ENC_TAIL signal is used to force the final encoder state to zero after being held high for 9 ECLK cycles. While ENC_TAIL is held high, the multiplexer in Figure 3 is in the "Tail" position, i.e., the input data is not selected.

For continuous data operation ENC_INIT and ENC_TAIL should be held low.

The 3GPP™ turbo code standard [2] has $g_0(D) = 1 + D^2 + D^3$ and $g_1(D) = 1 + D + D^3$. This is equivalent to G0I[2:1] = 10_2 and G1I[2:1] = 01_2. The 3GPP2 turbo code standard [3] has the same $g_0(D)$ and $g_1(D)$ as 3GPP, but with $g_2(D) = 1 + D + D^2 + D^3$ (G2I[2:1] = 11_2).

MAP Decoder

The MAP decoder is designed to be very flexible and can be operated in either continuous or block mode.

Theory of Operation

The MAP decoding algorithm [5] finds the following likelihood ratio:

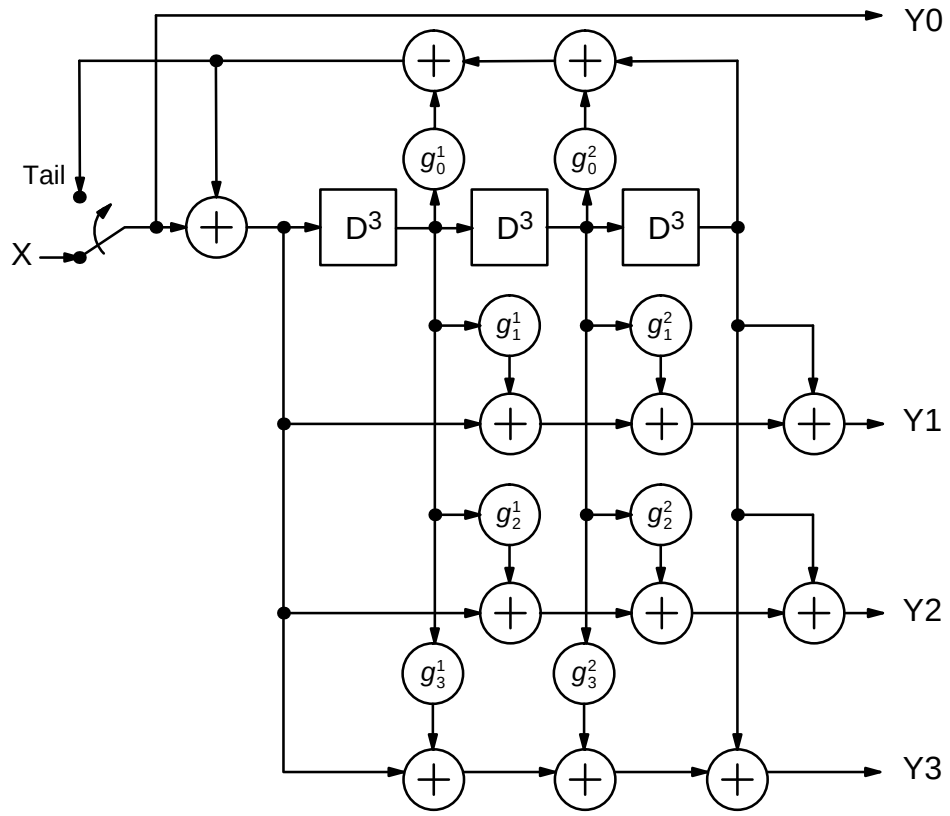

Figure 3: ENC03T triple interleaved 8 state systematic recursive convolutional encoder.

$$\lambda_k^0 = \frac{P_r(d_k = 1|R_1^N)}{P_r(d_k = 0|R_1^N)}, \quad (2)$$

where d_k is the encoded data bit at time k (equivalent to X in Figure 3) and R_1^N is the received data from time 1 to N. The basic algorithm for an additive white Gaussian noise (AWGN) channel involves exponentials, multiply–add, and division operations. By taking the negative logarithm of (2), the exponentials disappear, the multiplies becomes additions, the divisions become subtractions, and the additions become the E operand defined below:

$$a \text{ E } b = \min(a, b) - f(|a - b|) \quad (3)$$

where

$$f(z) = c \ln(1 + e^{-z/c}) \quad (4)$$

and c is a constant dependent on the signal amplitude and noise variance. The function $f(z)$ is implemented as look up tables within the decoder. When C4PIN and LOGMAP are both high, there are 18 integer values of c, from 0 to 17 via the C[4:0] inputs. C should be equal to the closest integer to c. For example, if c = 7.442, then C[4:0] = 7 $\equiv 00111_2$. Values of C greater than 17 are limited to 17. Due to quantisation effects, C = 1 is equivalent to C = 0.

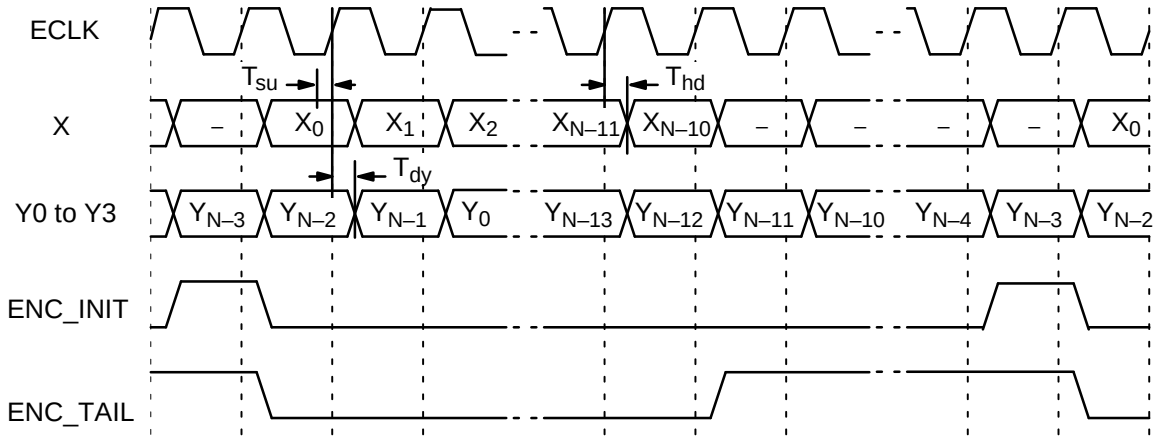

Figure 4: ENC03T Encoder Timing

When C = 0, $f(z) = 0$ and the sub–MAP (also known as max–log–MAP) algorithm is implemented [6]. The sub–MAP algorithm does not require knowledge of the signal to noise ratio (SNR), but does not perform as well as the MAP algorithm. The LOGMAP pin when low can also be used to select sub–MAP operation with greatly reduced decoder complexity.

Note that when a change in C is detected on a low–to–high transition of CLK, the decoder takes 67 CLK cycles for the new look–up tables to be loaded. If a change in C is detected during loading, the whole operation starts again.

When C4PIN and C4 are both grounded and LOGMAP is high, the maximum value of C is 9. This reduces the decoder complexity. The decoder takes 35 CLK cycles for the new look–up tables to be loaded. Note that C4PIN and LOGMAP are soft inputs and should not be connected to a pin.

We define the log–likelihood ratio as

$$L_k^0 = -c \ln \lambda_k^0. \tag{5}$$

For binary phase shift keying (BPSK) or quadrature phase shift keying (QPSK) modulation the received signal is described by

$$R_k^i = A((1 - 2y_k^i)/\sqrt{m} + n_k^i) \tag{6}$$

where A is the signal amplitude, $y_k^i \in \{0, 1\}$, $i = 0$ to 3 correspond to the coded bits, $m = 1$ for BPSK or $m = 2$ for QPSK, and n_k^i is a Gaussian distributed random variable with zero mean and normalised variance σ^2. For a systematic code $y_k^0 = d_k$. Figure 5 shows the signal sets for BPSK and QPSK. We have

$$\sigma^2 = \left(2mR\frac{E_b}{N_0}\right)^{-1} \tag{7}$$

where E_b/N_0 is the energy per bit to single sided noise density ratio and $R = k/n$ is the code rate (k is the number of information bits and n is the number of coded bits).

Since a zero is transmitted as $+A/\sqrt{m}$ and a one is transmitted as $-A/\sqrt{m}$ the sign bit of a noiseless R_k^0 in two's complement notation is equal to d_k. Similarly, (2) is formed so that the sign bit of L_k is equal to the estimate of d_k, i.e.,

$$\hat{d}_k = \begin{cases} 0 & : L_k \geq 0 \\ 1 & : L_k < 0 \end{cases}. \tag{8}$$

For optimal performance with BPSK or QPSK, the constant c should be adjusted such that

$$c = \sigma^2 \sqrt{m} A/2. \tag{9}$$

Due to quantisation and limiting effects the value of A should also be adjusted according to the received signal to noise ratio. A program for calculating the optimum values of A and c is freely available from [4].

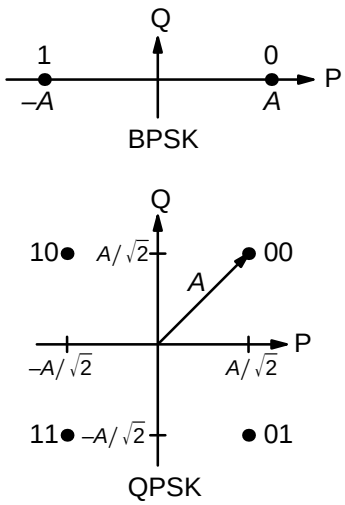

Figure 5: BPSK and QPSK signal sets.

The value of A directly corresponds to the 6–bit signed magnitude inputs (described in more detail later). The 6–bit inputs have 63 quantisation regions with a central dead zone. The quantisation regions are labelled from –31 to +31. For example, one could have $A = 15.7$. This value of A lies in quantisation region 16 (which has a range between 15.5 and 16.5).

Example 1: Rate 1/3 BPSK code operating at $E_b/N_0 = 0.3$ dB. From (7) we have $\sigma^2 = 1.39988$. Assuming c = 11 we have from (9) that $A = 15.7$.

Example 2: Rate 1/2 QPSK code operating at $E_b/N_0 = 0.8$ dB. From (7) we have $\sigma^2 = 0.41588$. Assuming c = 7 we have from (9) that $A = 23.8$. Note that the amplitude in each dimension is $A/\sqrt{2} = 16.8$.

A priori information corresponding to the information bit can also be input to the MAP decoder. This input corresponds to

$$Z_k^0 = -c \ln\left(\frac{P_r(d_k = 1)}{P_r(d_k = 0)}\right), \tag{10}$$

and is Z0I[7:0] in the MAP03T. The output L_k^0 (corresponding to L0O[7:0]) can be expressed as

$$L_k^0 = Z_k^0 + R_k^0 + Z_k^{0'}, \tag{11}$$

where $Z_k^{0'}$ is the extrinsic information.

The MAP03T also provides a log ratio output for the parity bits y_k^j, $1 \leq j \leq 3$ (equivalent to Yj in Figure 3). We define this as

$$L_k^j = -c \ln \frac{P_r(c_k = j|R_1^N)}{P_r(c_k = 0|R_1^N)} \tag{12}$$

which corresponds to LjO[7:0]. Similarly to L_k^0, we can express L_k^j as

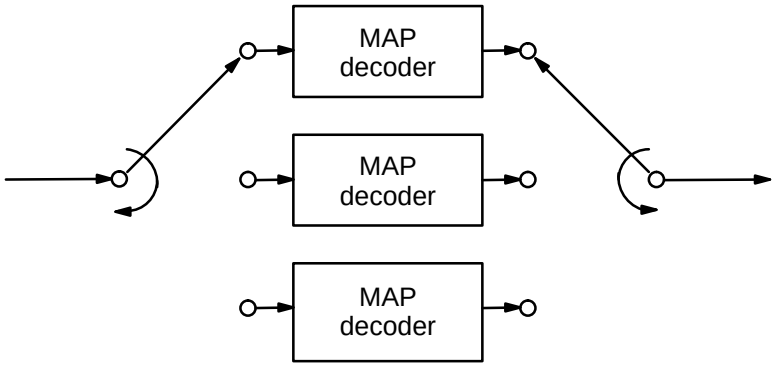

Figure 6: Equivalent triple interleaved MAP decoder.

$$L_k^j = Z_k^j + R_k^j + Z_k^{j\prime}, \qquad (13)$$

where Z_k^j is the *a priori* information for y_k^j, R_k^j is the received noisy parity symbol (RjI), and $Z_k^{1\prime}$ is the extrinsic information for y_k^1.

Decoder Operation

The MAP03T is a sliding block decoder [7] and is thus able to continuously decode data (just like a Viterbi decoder). This is achieved with a forward state metric calculator and two reverse state metric calculators that alternative in providing path metrics to the likelihood ratio calculator.

When SML_LRG_DEL is low or high the sliding block length (L) is 32 or 64, respectively. The decoding delay is 398 or 782 CLK cycles. For best performance an L of 64 should be chosen, especially when punctured codes are used. For minimum delay, L of 32 can be chosen.

The MAP03T also uses a unique triple interleaved architecture to maximise decoder speed. The equivalent decoder architecture is shown in Figure 6. Internally, the decoder is implemented as a single MAP decoder, but with three stages of pipelining. This allows a decoder speed that is nearly three times of what can normally be achieved with only a moderate increase in complexity.

The encoded and decoded streams are equivalent to three completely independent interleaved streams. Each equivalent MAP decoder has a decoding delay of $132^2/_3$ or $260^2/_3$ bits.

Block Operation

The decoder is also able to decode blocks of data with the same low decoder delay as in continuous mode. The static inputs BLK_START_0 and BLK_END_0 when high indicate whether the block starts or ends in state 0. When low the decoder assumes that the block starts or ends in an unknown state. The signals BLK_START and BLK_END indicate the start and end of the block in time. When these signals go high the forward and reverse state metrics of the MAP algorithm are initialised to their appropriate starting values. Figure 7 illustrates the timing for block encoded data. Note that only one of the triple interleaved schemes is using the BLK_START and BLK_END signals in this example.

Block codes with three parity bits can also be decoded. For these codes Y1 to Y3 are not used and R1I to R3I are set to 0. The divisor polynomial g_0 should be a primitive polynomial such as $g_0 = 1 + D^2 + D^3$ (G0I[2:1] = 10_2). Block encoding and decoding is performed as normal (the encoder and decoder states must be made to both start and end in state zero). The (7,4) BCH code

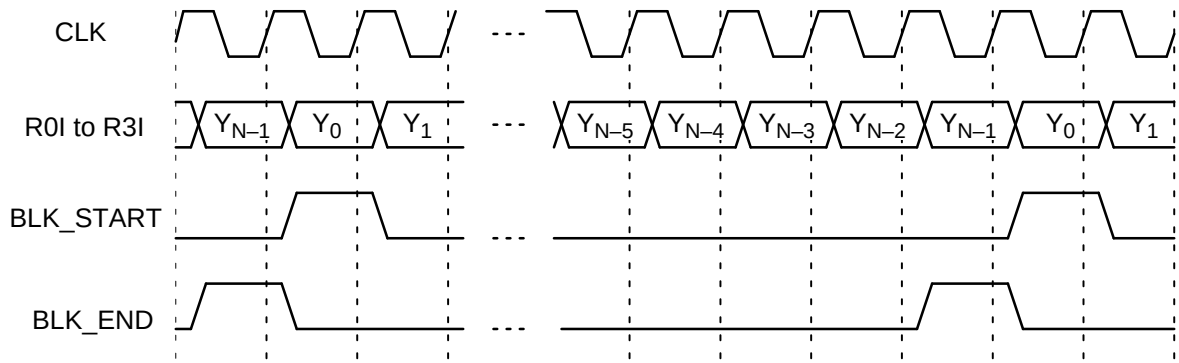

Figure 7: Decoder Block Timing

is a block code that can be near–optimally decoded. Shorter or longer block lengths are also possible.

Data Formats

When RZ is low, the seven bit received data R0I to R3I can be in signed magnitude or two's complement format. In signed magnitude format (SMG_TCM low), the most significant bit (i.e., RiI6, i = 0 to 3) corresponds to the sign bit and the remaining bits represent the magnitude. When SMG_TCM is high the input data is in two's complement format. Table 2 gives a partial listing of the range represented by each quantised value.

Internally, the decoder converts the seven bit R0I to R3I values to six bit signed magnitude quantisation with a central dead zone. Table 3 shows the six bit internal quantisation ranges. For external six bit signed magnitude data with central dead zone quantisation, the data is input to RiI[6:1] with RiI0 = 0. For six bit two's complement data with central dead quantisation, the data is input to RiI[6:1] with RiI0 = RiI6.

Internally, Z0I is added to R0I to produce an eight bit signed magnitude value.

Table 2: Quantisation for R0I to R3I.

Sign Mag.	Two's Comp	Range
63	63	63↔∞
62	62	62↔63
⋮	⋮	⋮
1	1	1↔2
0	0	0↔1
64	127	–1↔0
65	126	–2↔–1
⋮	⋮	⋮
126	65	–63↔–62
127	64	–∞↔–63

When RZ is high REi,RiI[6:0] for i = 1 to 3 are equal to eight bit two's complement inputs with notation Z1I[7:0] to Z3I[7:0]. Internally, Z1I to Z3I are converted to eight bit signed magnitude values. This allows the decoder to iteratively decode serially concatenated convolutional codes. In this case, the inner decoder has RZ low and the outer decoder has RZ high. For iteratively decoding parallel concatenated codes, RZ is low for both the inner and outer decoders.

The eight bit Z0I to Z3I inputs and L0O to L3O outputs are in two's complement arithmetic. Table 4 gives a partial listing of the range represented by each quantised value.

Table 3: Internal quantisation for R0I to R3I.

Decimal	Binary	Range
31	011111	30.5↔∞
30	011110	29.5↔30.5
⋮	⋮	⋮
2	000010	1.5↔2.5
1	000001	0.5↔1.5
0	000000	–0.5↔0.5
32	100000	–0.5↔0.5
33	100001	–1.5↔–0.5
34	100010	–2.5↔–1.5
⋮	⋮	⋮
62	111110	–30.5↔–29.5
63	111111	–∞↔–30.5

For rate 1/2 codes and MODE = 7 (see next section), REi,RiI[6:0] for i = 0 to 3 are equal to eight bit branch metric (BM) inputs with notation BM0I[7:0] to BM3I[7:0]. RZ, SMG_TCM, and Z0I inputs are not used. The BM inputs correspond to the BM's for symbols $2y^1 + y^0$, e.g., the BM for $y^1 = 1$ and $y^0 = 0$ corresponds to BM2I. The BM's range in value from 0 to 255. The lower the BM value, the more likely the symbol. To maximise performance, the smallest BM should be subtracted from all four BM's (implying that the smallest BM will then be equal to zero).

Table 4: Quantisation for Z0I to Z3I and L0O to L3O.

Decimal	Binary	Range
127	01111111	127↔∞
126	01111110	126↔127
⋮	⋮	⋮
1	00000001	1↔2
0	00000000	0↔1
255	11111111	–1↔0
254	11111110	–2↔–1
⋮	⋮	⋮
129	10000001	–127↔–126
128	10000000	–∞↔–127

The branch metric inputs can be used to decode signal sets other than BPSK and QPSK, e.g., rate 1/2 16QAM. For these signal sets, the branch metrics are not linear to the received signal. Non–linear computations or look–up tables

can be used to calculate the branch metrics for these signal sets.

Punctured Code Operation

When RZ is low, the input signals RE0 to RE3 are used to enable the received data inputs R0I to R3I, respectively. Data is erased when RE0 to RE3 are low for use in punctured code decoding. Manual puncturing can be performed by forcing R0I[5:0] to R3I[5:0] low.

Example 3: Rate 1/2 code punctured to rate 2/3. In this case the systematic bit is not punctured (RE0 high) while the parity bit is punctured every second bit (RE1 alternates between high and low). RE1 is equal to CLK divided by six. The phase of RE1 needs to match the received data so that when RE1 is low, the parity information is punctured.

Mode Selection

To minimise the decoder complexity, the MODE[2:0] inputs can be used with the schematic symbols to select only those rates and input types that are expected to be used. Table 5 gives the number of slices for Virtex, Virtex–E, Spartan–II, and Spartan–IIE devices for the ten possible modes of operation. The number of slices for Virtex–II devices is about 6 to 18 slices less. Table 6 gives the number of BlockRAMs that are used.

Table 5: Slices (Virtex)

Mode	n	Input	LOGMAP/C4PIN		
			LL	HL	HH
0	1	R	1080	1454	1711
1	2	R	1144	1518	1775
2	3	R	1326	1700	1957
3	4	R	1428	1802	2059
4	2	R,Z	1411	1918	2252
5	3	R,Z	1767	2407	2818
6	4	R,Z	2128	2901	3389
7	2	BM	1248	1622	1879
8	4,2	R,BM	1571	1945	2202
9	4,2	R,Z,BM	2229	3002	3490

The first column gives the decoder mode selected by MODE[2:0]. The second column gives the number of code bits *n*. The third column gives the input type; R for received data, Z for a priori data, and BM for branch metric data.

The next three columns gives the number of slices for the three different decoding algorithms. This is indicated by the LOGMAP/C4PIN configuration. The first of the three columns is for sub–MAP operation (LOGMAP = C4PIN = L). In this case C[4:0] is not used. The second of the three columns is log–MAP with a maximum C of 9 (LOGMAP = H and C4PIN = L). In this case input C4 should not be connected to a pin. The third of the three columns is log–MAP with a maximum C of 17 (LOGMAP = C4PIN = H).

Table 6: BlockRAMs

Mode	n	Input	Virtex	Virtex–II
0	1	R	6	3
1	2	R	7	4
2	3	R	9	4
3	4	R	10	5
4	2	R,Z	7	4
5	3	R,Z	9	4
6	4	R,Z	10	5
7	2	BM	10	5
8	4,2	R,BM	10	5
9	4,2	R,Z,BM	10	5

Note that LOGMAP and C4PIN are soft inputs and should be connected to internal VCC and GND supplies. Not doing so will result in excessive complexity and decreased decoder speed.

For modes 0 to 7, MODE[2:0] is directly equal to the mode number, e.g., for mode 4, MODE[2:0] = 100_2. Except for the following two cases, MODE[2:0] are soft inputs and should be connected internal VCC and GND supplies.

For mode 8, MODE2 should be connected to an input pad while MODE1 and MODE0 should be connected to VCC. MODE2 can then be used to select between R inputs with $n = 4$ (MODE2 low) and BM inputs with $n = 2$ (MODE2 high).

For mode 9, MODE0 should be connected to an input pad while MODE1 and MODE2 should be connected to VCC. MODE0 can then be used to select between R or Z inputs with $n = 4$ (MODE0 low) and BM inputs with $n = 2$ (MODE0 high).

For R inputs, only L0O is output. For R,Z inputs all the outputs are provided corresponding to the number of inputs. Table 7 shows the various inputs and outputs that are available for BIT/MCS files for the ten different modes. Both the encoder and decoder use the same G inputs.

If the code selection inputs G0I to G3I are connected to pins, decoder complexity increases by approximately 10–20%.

The DCS input when low puts the decoder into a low power mode. The RST input when high synchronously resets the decoder. For BIT/MCS files, these inputs are not connected to pins with DCS = H and RST = L.

Table 7: Inputs and outputs selected for BIT/MCS files for different modes

Inputs and Outputs	Mode									
	0	1	2	3	4	5	6	7	8	9
BLK_END, BLK_END_0, BLK_START, BLK_START_0, CLK	●	●	●	●	●	●	●	●	●	●
RESET, ECLK, ENC_INIT, ENC_TAIL, X, SML_LRG_DEL	●	●	●	●	●	●	●	●	●	●
C[4:0]*	●	●	●	●	●	●	●	●	●	●
RE0, R0I[6:0], Y0, L0O[7:0]	●	●	●	●	●	●	●	●	●	●
RE1, R1I[6:0], Y1		●	●	●	●	●	●	●	●	●
RE2, R2I[6:0]			●	●		●	●	●	●	●
Y2			●	●		●	●		●	●
RE3, R3I[6:0]				●			●	●	●	●
Y3				●			●		●	●
L1O[7:0], RZ					●	●	●			●
L2O[7:0]						●	●			●
L3O[7:0]							●			●
MODE0/MODE2									●	●
SMG_TCM, Z0I[7:0]	●	●	●	●	●	●	●		●	●

* C[4:0] not connected if LOGMAP low, C4 not connected if C4PIN low

Switching Characteristics

The following switching characteristics reflect worse–case values over the recommended operating conditions. The values are expressed in units of nanoseconds. All values are preliminary.

SW–MAP03T1C4–XCV200E–8PQ240C		–6		–7		–8	
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Signal setup before CLK, ECLK	T_{su}	1.5		1.4		1.3	
Signal hold after CLK, ECLK	T_{hd}	0		0		0	
Signal delay after CLK, ECLK	T_{dy}		2.9		2.8		2.4
ECLK period	T_{ecp}	5.79		5.23		4.66	
CLK period	T_{cp}	14.39		12.85		9.99	
CLK low	T_{clh}	2.4		2.1		1.9	
CLK high	T_{wps}	2.4		2.1		1.9	

SW–MAP03T1C4–XC2V500–5FG256C		–4		–5		–6	
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Signal setup before CLK, ECLK	T_{su}	1.11		0.96		0.88	
Signal hold after CLK, ECLK	T_{hd}	–0.45		–0.39		–0.36	
Signal delay after CLK, ECLK	T_{dy}		3.44		2.99		2.72
ECLK period	T_{ecp}	7.67		6.67		6.07	
CLK period	T_{cp}	10.44		9.08		8.25	
CLK low	T_{clh}	0.77		0.67		0.61	
CLK high	T_{wps}	0.77		0.67		0.61	

Example

In this section we give an example of how the MAP03T can be used as a continuous rate 1/2 QPSK encoder and decoder. Note that the MAP03T does not perform any synchronisation. This needs to be performed external to the chip.

A simple synchronisation circuit could monitor the output magnitude of the decoder output. The average magnitude will be higher in the synchronised state compared to the unsynchronised states.

Figure 8 shows how the MAP03T1C4 (1 indicates the mode and C4 indicates that pins C[3:0] are used) can be configured for continuous rate 1/2 QPSK operation. The code used is $g_1 = 15_8 = 1101_2 \rightarrow$ G1I[2:1] = 10_2 = 2 and $g_0 = 13_8 = 1011_2 \rightarrow$ G0I[2:1] = 01_2 = 1 (which is 180° rotationally invariant). Note that unconnected inputs are pulled down to ground. Since the code is invariant to 180° phase rotations, differential encoding and decoding can be used if desired.

The demodulator output is assumed to be in two's complement form. An *L* of 64 is used for best performance. The information and parity bits are assumed to be equally likely implying Z0I = 0. Unconnected inputs are pulled to ground.

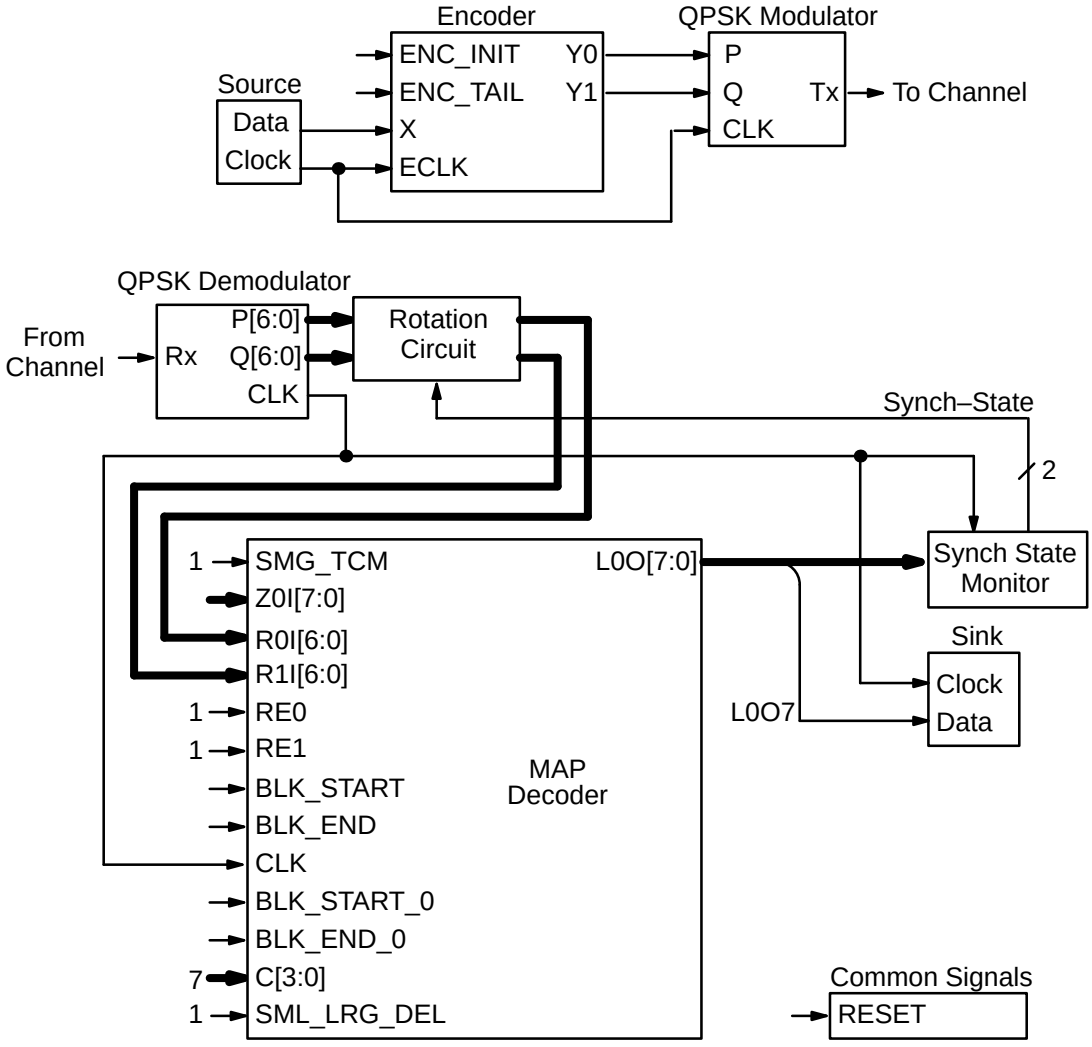

Figure 8: Block diagram of rate 1/2 QPSK codec.

BIT and MCS Files

The BIT file is what is downloaded into the FPGA on startup. The Xilinx data book explains how this can be achieved. The MCS files can be used to program serial PROMs which can then be used to program the FPGA on powerup.

For the BIT files, the encoder and decoder are asynchronously reset when RESET (not shown in schematic symbols) goes high. Except for clock inputs, all the inputs for the encoder and decoder have pulldown resistors.

Configuration

This section gives the options that were selected for Virtex–E and Virtex–II devices.

Configuration (Virtex/Virtex–II)

- Configuration Rate: 4 MHz
- Configuration Pins –
  Configuration Clk: PullUp
  M0: PullUp
  M1: PullUp
  M2: PullUp
  Program: PullUp
  Done: PullUp
  Unused Pins: PullUp
- JTAG Pins –
  TCK: PullUp
  TDI: PullUp
  TDO: Float
  TMS: PullUp
- Produce ASCII Configuration File: No
- Enable the User ID Code: Yes
  Code: 53570202_H (MAP03T02)
  53570203_H (MAP03T03)
- Enable .bit File Compression: No

Configuration (Virtex–II)

- Perform a Cyclical Redundancy Test: Yes
- Enable DCM Shut Down (reset): No
- Disable All DCMs: No

Startup

- Start–Up clock: CCLK
- Output Events –
  Done: C4
  Enable Outputs: C5
  Release Set/Reset: C6
  Release Write Enable: C6 (Virtex)
  Release Write Enable: No Wait (Virtex–II)
  Release DLL: No Wait
  Hold for DCI: No Wait (Virtex–II)
- Enable Internal Done Pipe: No

Readback

- Configuration Mode: JTAG
- Security –
  Enable Readback and Reconfiguration: Yes
  Generate Readback Bit Stream: No
  Disable Readback: No
  Disable Readback and Reconfiguration: No

Pinouts (Virtex–E/Virtex–II)

Pad Name	PQ240	FG256
BLK_END	P208	F2
BLK_END_0	P149	M10
BLK_START	P100	L12
BLK_START_0	P147	M2
CLK	P92	A9
C0	P52	J4
C1	P50	J3
C2	P65	K3
C3	P49	K4
C4		
ECLK	P89	D8
ENC_INIT	P84	T10
ENC_TAIL	P74	P10
L0O0	P186	P8
L0O1	P175	N8
L0O2	P199	M1
L0O3	P192	N1
L0O4	P191	T7
L0O5	P195	M4
L0O6	P194	P1
L0O7	P193	T8
L1O0		
L1O1		
L1O2		
L1O3		
L1O4		
L1O5		
L1O6		
L1O7		
R0I0	P35	J1
R0I1	P39	L1
R0I2	P36	L4
R0I3	P66	M6
R0I4	P67	L2
R0I5	P68	L5
R0I6	P27	T11
R1I0	P222	T6
R1I1	P223	T5
R1I2	P218	M7
R1I3	P217	G3
R1I4	P221	H4
R1I5	P220	H3
R1I6	P228	J2
RE0	P40	L3
RE1	P224	H2
RESET	P238	H1
RZ		
SMG_TCM	P229	L16
SML_LRG_DEL	P168	M11
X	P80	G2
Y0	P78	K2
Y1	P79	G4
Z0I0	P70	N7
Z0I1	P71	N10
Z0I2	P72	T9
Z0I3	P38	N9
Z0I4	P33	R9
Z0I5	P34	P9
Z0I6	P31	R8
Z0I7	P26	P7

Please consult the Xilinx data book for power and configuration pinouts.

Packages

UCF No.	Mode	Xilinx Part No.
MAP03T02	1C4	XCV200E–8PQ240C
MAP03T03	1C4	XC2V500–5FG256C

Other Xilinx parts and modes are also available. All pinouts are upward compatible. See the Xilinx data book for pinouts of other packages. Other pinouts can be ordered from *Small World Communications*.

Ordering Information

SW–MAP03T–UNL for EDIF/VHDL core yearly unlimited license

SW–MAP03T–BAS–*n* for EDIF/VHDL core basic license

SW–MAP03T–*m*C*c*–*p*–*n* for BIT/MCS file

n = number of instantiations

m = mode (0 to 9)

c = no. of C pins (0 for LOGMAP low, 4 for LOGMAP high and C4PIN low, or 5 for LOGMAP high and C4PIN high)

p = Xilinx part no. (e.g., XCV200E–8PQ240C)

For BIT/MCS files, the default code is compatible with the 3GPP™ and 3GPP2 standards ($g_0 = 13_8$, $g_1 = 15_8$, $g_2 = 17_8$, $g_3 = 11_8$). If you wish to use a different code, please indicate this in your order.

For basic core and bit file licenses, please indicate how many instantiations you wish to license. An instantiation is considered to be an integrated circuit that uses or is derived from our software in the device's programming or manufacture. License costs per instantiation decrease with increasing number of instantiations. Yearly, unli-

mited instantiation licenses are also available. Note that *Small World Communications* only provides software and does not provide the actual devices themselves. Please contact *Small World Communications* for a quote on the number of instantiations and type of license you require.

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