LCE01C Features

LDPC Encoder

- CCSDS compatible
- Rate 223/255 (8160,7136)
- Up to 250 MHz internal clock
- Up to 1.75 Gbit/s input data rate
- 8–bit byte input and output
- Xilinx LUTs: 12.3K Spartan 3 and Virtex–4, 9.2K Virtex 5, Virtex 6, Spartan 6 and 7–Series. Altera ALUTs 10.2K.

- Available as EDIF core and VHDL simulation core for Xilinx Virtex–II, Spartan–3, Virtex–4, Virtex–5, Virtex–6, Spartan–6 and 7–Series FPGAs under SignOnce IP License. Actel, Altera and Lattice FPGA cores available on request.
- Available as VHDL core for ASICs
- Low cost university license also available

Introduction

The LCE01C is a fully compatible CCSDS rate 223/255 (8160,7136) LDPC [1] error control encoder. A regular quasic–cyclic LDPC code with 511x511 square circulants with weight 2 in the parity check matrix is used. There are 2x16 circulants, resulting in a check node degree of 32 and a variable node degree of 4.

Figure 1 shows the schematic symbol for the LCE01C encoder. The EDIF core can be used with Xilinx Integrated Software Environment (ISE) software to implement the core in Xilinx FPGA's. The VHDL core can be used in ASIC designs.

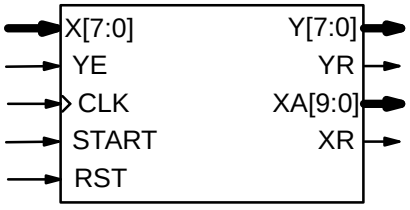

Figure 1: LCE01C schematic symbol.

Table 1 shows the performance achieved with various Xilinx parts. T_{cp} is the minimum clock period over recommended operating conditions. These performance figures may change due to device utilisation and configuration.

Table 1: Performance of Xilinx parts.

Xilinx Part	T_{cp} (ns)	Mbit/s
XC3S1000–4	11.237	621
XC3S1000–5	9.850	708
XC6SLX25–2	8.487	822
XC6SLX25–3	7.510	929
XC4VLX15–10	5.903	1182
XC4VLX15–11	5.034	1386
XC4VLX15–12	4.468	1561
XC5VLX30–1	6.101	1143
XC5VLX30–2	5.248	1329
XC5VLX30–3	4.680	1491
XC6VLX75T–1	5.098	1368
XC6VLX75T–2	4.437	1572
XC6VLX75T–3	3.995	1746
XC7A100T–1	5.915	1179
XC7A100T–2	4.827	1445
XC7A100T–3	4.295	1624
XC7K70T–1	5.435	1283
XC7K70T–2	4.436	1572
XC7K70T–3	4.000	1744

Signal Descriptions

CLK	System Clock
RST	Synchronous Reset
START	Encoder Start
X	Data In
XA	Data In Address
XR	Data In Ready
Y	Data Out
YE	Data Out Enable
YR	Data Out Ready

Encoder

Figure 2 gives a block diagram of the LCD01C encoder. X is the data input and Y is the coded output. Data is clocked during the low to high transition of CLK.

The data is input eight bits at a time in the sequence $X_k = \{x_{8k},...,x_{8k+7}\}$ from time $k = 0$ to $K/8–1$, where $K = 7136$. That is, the first bit of the first data symbol X[7:0] to be encoded is the most significant bit X[7]. Similarly, the first bit of the first

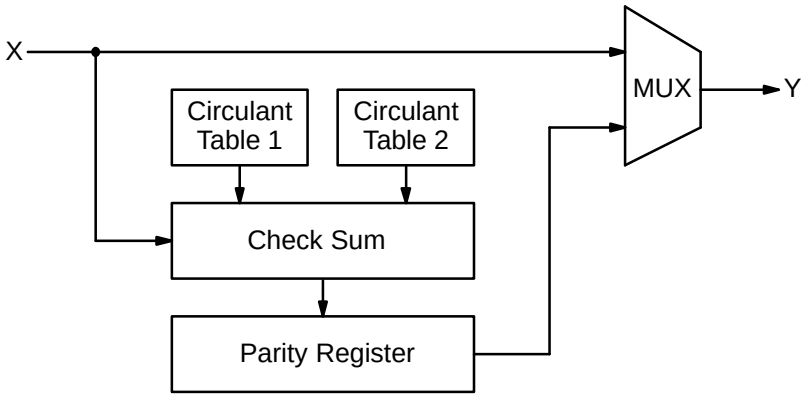

Figure 2: LCE01C Systematic Encoder.

encoded symbol Y[7:0] to be transmitted is the most significant bit Y[7].

As 8 is not a factor of the circulant size of 511, this implies that two circulant tables are required. One circulant table is used when all eight inputs select rows within one circulant. Two tables are used when the eight inputs stradle two circulants.

While data is entered, the output Y selects the input data X. After the data is input, the output Y selects the parity register for $(N–K)/8 = 128$ clock cycles.

Note that the output is one continuous stream. The encoder does not pause (unless YE goes low) in outputting the data. If YE goes low, then the input data must be held.

Figure 3 shows the initial timing diagram. When the encoder requires data X to be read from the input RAM, the data ready signal XR goes high and XA[9:0] selects the data byte. After a START signal is initiated XR goes high after one cycle. It is assumed that the data is stored in a synchronous read RAM. The signals XR and YE can be used to control the enable input of the RAM. An asynchronous read RAM can also be used by registering the RAM output. Input data X only needs to be valid when YE is high.

If YE is high, the encoded data ready signal YR goes high three clock cycles after a START signal is initiated. YR is high for both the data block and parity. If YE is low the encoder is held during the next low–to–high transition of CLK.. Figure 4 shows the encoding process for the parity. It is assumed that the first transmitted bit is $Y_0[7]$.

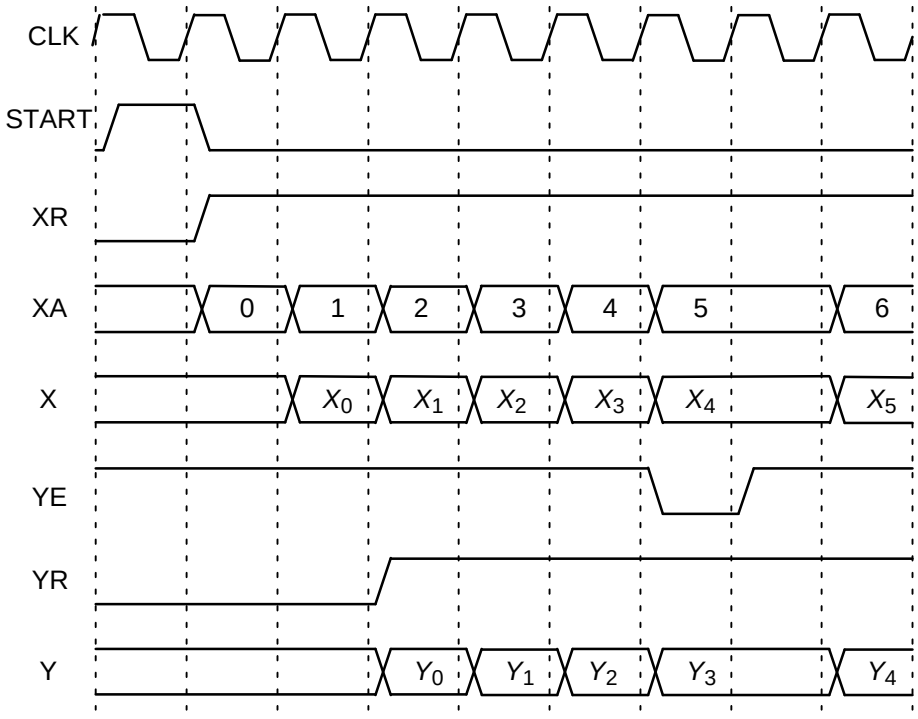

Figure 3: LCE01C Initial Encoder Timing.

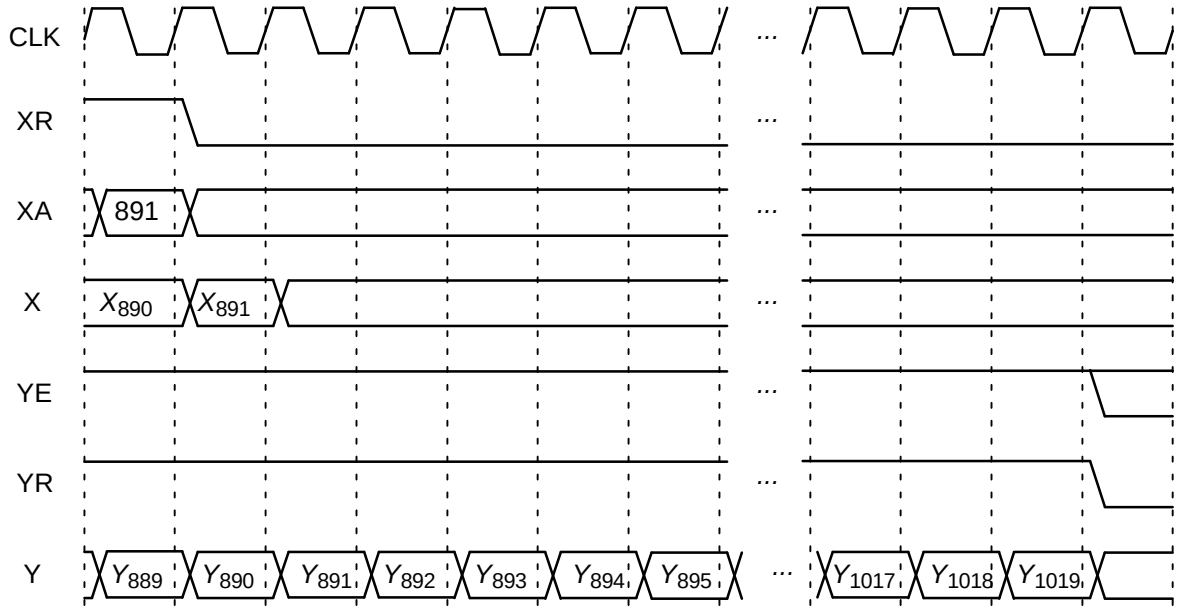

Figure 4: LCE01C encoder parity timing.

The nominal input data rate f_e is

$$f_e = \frac{f_E K}{N/8 + 3} \quad (1)$$

where $f_E = 1/T_{cp}$ is the encoder clock speed. For the (8160,7136) code, this results in $f_e = 6.98 f_E$.

Ordering Information

SW–LCE01C–SOS (SignOnce Site License)
SW–LCE01C–SOP (SignOnce Project License)
SW–LCE01C–VHD (VHDL ASIC License)
SW–LCE01C–UNI–n (University License)

All licenses include EDIF and VHDL cores. The VHDL cores can only be used for simulation in the SignOnce and University licenses. The University license is only available to tertiary educational institutions such as universities and colleges and is limited to n instantiations of the core. The SignOnce and ASIC licenses allows unlimited instantiations.

Note that *Small World Communications* only provides software and does not provide the actual devices themselves. Please contact *Small World Communications* for a quote.

References

[1] Consultive Committee for Space Data Systems, “TM synchronization and channel coding,” CCSDS 131.0–B–2, Aug. 2011.

Small World Communications, 6 First Avenue, Payneham South SA 5070, Australia.
info@sworld.com.au ph. +61 8 8332 0319
http://www.sworld.com.au fax +61 8 8332 3177

Revision History

- v0.00 20 August 2012. Preliminary product specification.
- v1.00 27 March 2013. Added Xilinx performance and complexity.